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Thermal oxidation of lattice matched InAlN/GaN heterostructures

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In this work we have investigated the thermal oxidation of thin InAlN/GaN heterostructures in their lattice matched configuration (83% Al) in oxygen atmosphere at 800 °C. TEM cross sections revealed a partially crystalline oxide with an initial oxidation rate of 0.37 nm/minute. MOS diodes fabricated using the thermal oxide as a gate dielectric showed an exponential drop in the gate leakage which scales with the square root of oxidation time indicating diffusion limited oxidation through the InAlN barrier. The effect of oxidation on the interfacial InAlN/GaN sheet charge density (NS) is correlated with a reduction of thickness for short oxidation times (up to 4 min) and an abrupt change in the surface potential for longer oxidation times.

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1 Introduction GaN heterostructures are highly polar and surface properties play an important role in their intrinsic charge balance, where surface states act as deep donors. Such surface donor states may be avoided at the InAlN surface when inserting a thin dielectric interlayer between the semiconductor barrier material and at the same time the FET gate leakage is reduced. $In_{0.83}Al_{0.17}N$/GaN High electron Mobility Transistors (HEMT's) in their lattice matched configuration represent an alternative to AlGaN/GaN HEMT's, with high 2DEG channel charge density [1] and thermal stability above 1000°C in the lattice matched configuration [2] even for ultra thin layers down to 3 nm [3]. However, due to the thin InAlN barrier used, these devices have often suffered from high gate leakage current. The gate leakage can be reduced by inserting a thin dielectric layer under the gate, realized by CVD deposition [4]. An alternative approach will be the utilization of the heterostructures high thermal stability to introduce a thin native oxide as dielectric by thermal oxidation at 800 °C in oxygen atmosphere [5]. In the later approach an InAlN/GaN MOSHEMT prepared by thermal oxidation proved the suitability of the thermal oxide for FET applications. A deeper understanding of the nature of the oxide and the oxidation process is needed to optimize this process.

The thermal oxidation mechanism and its effect on the heterostructure electrical properties were investigated by High Resolution TEM (HRTEM) cross sections and MOS-diode structures.

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2 Experiment The structure studied here was grown by MOCVD system on a 2 inch diameter SiC substrate. The structure consists of 1.7 µm thick GaN buffer, 1 nm thick AlN spacer layer and variable InAlN barrier layers ranging from 6 to 15 nm in thickness, with 83% Al content. MOS-diodes were realized as follows: The devices are mesa isolated by Ar plasma etching. Then, Ti/Al/Ni/Au ohmic contact stacks are alloyed at 890°C in nitrogen atmosphere. Blanket thermal oxidation of the whole surface was conducted at 800 °C in oxygen atmosphere for different times of oxidation. Ni/Au is deposited to produce the gate diode contacts (50 µm x 0.25 µm). A cross section of the MOS-diode is shown in Fig. 1. TEM cross sections of oxidized layers were used to determine the oxide thickness and material properties. DC measurements were conducted to determine the diode characteristics.

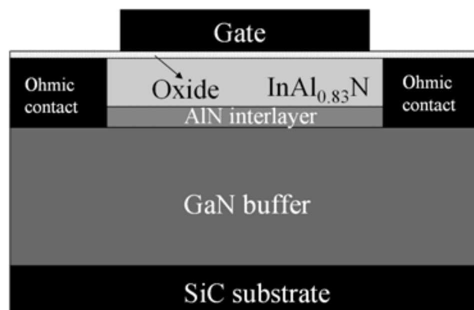

Figure 1 Cross section of InAlN/GaN MOS-diode prepared by thermal oxidation at 800 °C in oxygen atmosphere.

3 Results and discussion High-Resolution TEM cross sections of the heterostructure with 10 nm InAlN barrier prior and after 4 and 8 minutes of oxidation is shown in Fig. 2. Figure 2b shows that after 4 minutes of oxidation the resulting native oxide film is crystalline and has a sharp flat interface to the InAlN. After 8 minutes of oxidation (Fig. 2c) the oxide still preserves its crystalline structure, but in this case the interface to the InAlN is significantly rougher probably due to a composition variations or induced stress in the InAlN. Further investigation on the exact structural and morphological change will be carried out. The initial oxidation rate inferred from these images is 0.37 nm/min.

With such ultra thin InAlN barriers it is expected that the dominant current leakage mechanism in a diode is the tunnelling mechanism. As in the case of Silicon, insertion of a thin dielectric would reduce the leakage current (I_0) exponentially with oxide thickness as described in Eq. (1) below [6,7]:

$$I_o \propto C_1 \frac{V_0}{t_{ox}}.\exp\left(-C_2 \frac{t_{ox}}{V_0}\right) \qquad (1)$$

Where C_1 and C_2 are material related constants, t_{ox} is the thickness of the oxide and V_0 is the voltage across the tunnelling barrier. Moreover; the thickness of the oxide for a diffusion limited oxidation mechanism is proportional to the square root of time as described in Eq. (2) below [8]:

$$t_{ox} \approx \sqrt{Bt} \qquad (2)$$

where t is the oxidation time and B is the parabolic rate constant. From Eq. (1) and Eq. (2) the logarithm of the leakage current is linearly dependent on the square root of oxidation time.

Similar behaviour is observed for 6 nm InAlN barrier MOS-diodes prepared with thermal oxidation. Figure 3.a shows the gate diode characteristics of a 6 nm InAlN barrier MOS-diode oxidized for 2 and 5 minutes compared to a Schottky type diode. As can be seen in the figure, an exponential drop of the leakage current is observed with increased oxidation time. Recording the current values at a chosen gate source voltage (V_0), -20 V in this case, and plotting it with the square root of oxidation time reveals a linear dependence (see Fig. 3b), which indicates initially diffusion limited oxidation mechanism similar to the case of Silicon.

With the thickness data of the formed oxide from Fig. 2b the estimated parabolic rate constant (B) of the oxidation is 5.7 x 10^{-15} cm^2/min.

To correlate the effect of oxidation with the intrinsic properties of the heterostructure, namely the sheet charge density (N_S), the structure shown in Fig. 1 was fabricated up to the ohmic contacts step. The device was oxidized for different times, while shielding the ohmic contact metals

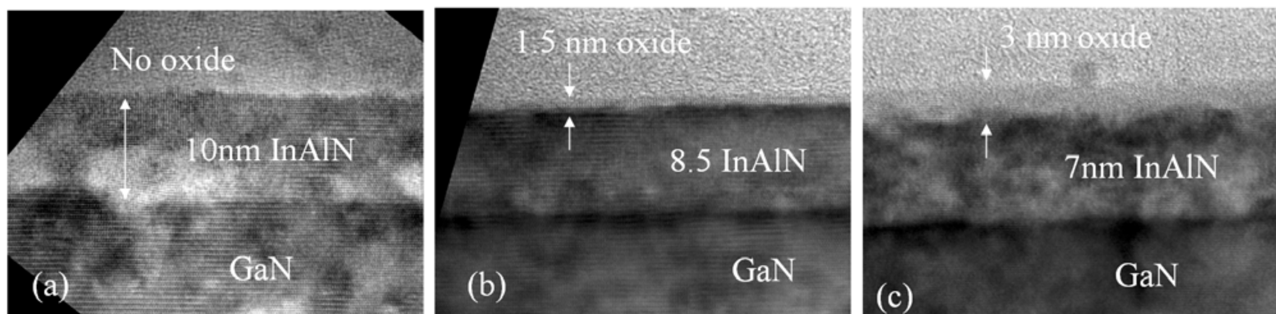

Figure 2 HRTEM cross sections of 10 nm InAlN/GaN (a) prior to thermal oxidation (b) after 4 minutes and (c) 8 minutes of thermal oxidation at 800 °C in oxygen atmosphere.

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with a Si_3N_4 mask. The drop in the saturated current density (I_{DS}) relative to the saturated current density prior to oxidation (I_{DS0}) was recorded (see Fig 4). In this case the drop in I_{DS} is directly proportional to a drop in N_s. The drop in I_{DS} is relatively slow for oxidation times up to 4 minutes (denoted step I in the figure) but increases abruptly after up to 20 minutes of oxidation (denoted step II in the figure) and relaxes again to a slow rate for longer times, which may indicate a self limiting oxidation.

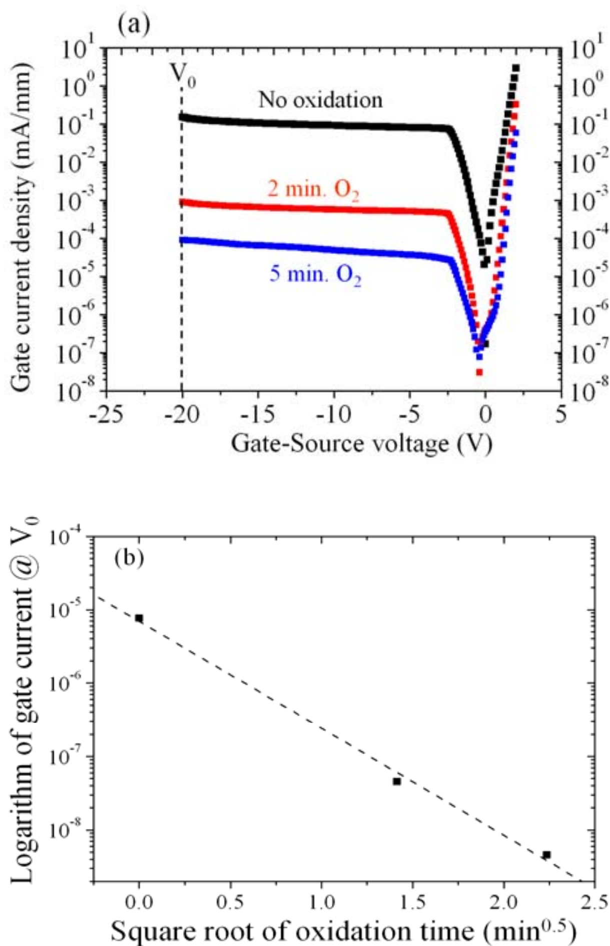

Figure 3 6 nm InAlN barrier MOS-diode characteristics prepared by thermal oxidation at 800 °C in O_2 atmosphere compared to a Schottky type diode. (b) The square root behaviour of the oxidation mechanism.

The data described in Fig. 4 and the residual InAlN thicknesses shown in Fig. 2 are correlated together to give insight on the factors changing N_s with oxidation time. Simulated data of N_s as a function of the barrier thickness and the surface potential are shown in Fig. 5. These simulations were conducted using a Poisson-Schrödinger equation solver. The best fit to experimental Hall measurement data of different InAlN barrier thicknesses is a surface potential of 0.6 eV. Details can be found in [8]. The InAlN thickness data from TEM and I_{DS}/I_{DS0} data from the experiment are overlaid on the surface potential curves assuming an I_{DS}/I_{DS0} to N_s/N_{s0} ratio of 1 to 1.

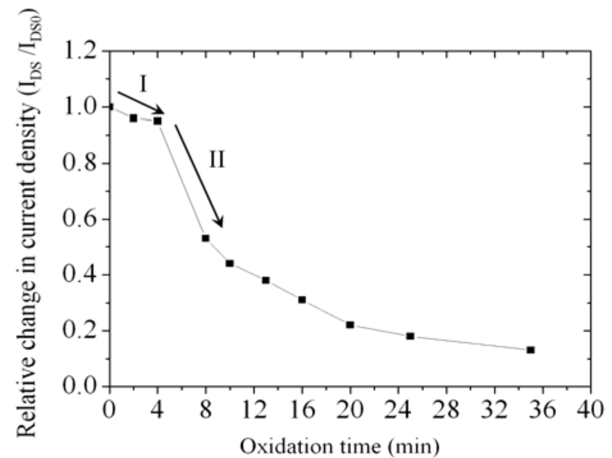

Figure 4 Saturated current density drop as a function of oxidation time.

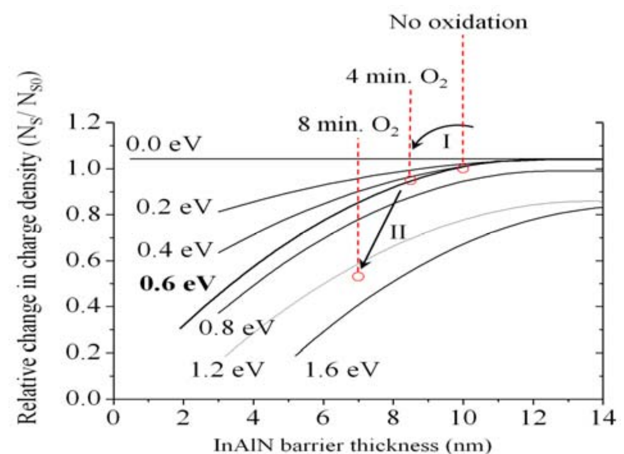

Figure 5 Simulated N_S vs. the surface potential and the InAlN barrier thickness. Drop in N_S occurs when (I) the barrier thickness is reduced while maintaining a relatively constant surface potential for short oxidation times and (II) an abrupt change in the surface potential for longer times.

During the first few minutes of oxidation the drop in N_s is correlated with a reduction of the InAlN barrier thickness with no or minor change of the surface potential (denoted step I in Fig. 5), after that an increase in the surface potential up to about 1.1 eV causes the sudden drop in N_S (denoted step II in Fig. 5). This drop in the surface potential could be caused by a change in the composition or added stress to the InAlN layer as discussed earlier. These results highlight an important trade-off between the drop of leakage current that can be achieved with oxidation time (at 800 °C) and the drop in N_s that reflects on the current density of the device.

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4 Conclusion Despite the rare applicability of thermal oxidation of III-Nitrides, the lattice matched InAlN/GaN heterostructure have been thermally oxidized at 800 °C in oxygen atmosphere resulting in the insertion of a thin native oxide that can be used as a gate dielectric to reduce the gate leakage current. This oxide is crystalline and the oxide thickness is controlled by the oxidation time due to the relatively slow initial oxidation rate. The oxidation mechanism seems to be diffusion limited with a dependence on the square root time of oxidation similar to the case of Si oxidation. First order approximations deduced from TEM images and MOS-diode measurements yielded an initial oxidation rate of 0.37 nm/min with a parabolic rate constant of 5.7×10^{-15} cm^2/min. The effect of the oxidation on both the surface potential and the remaining InAlN barrier thickness gives a limit to the tolerable oxidation time that will produce an effective gate dielectric without sacrificing the carrier density. To further optimize the oxidation process experiments with different oxidation temperatures and atmospheres should be conducted.

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