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Highly-Ordered 3D Vertical Resistive Switching Memory Arrays with Ultralow Power Consumption and Ultrahigh Density

Ahmed Al-Haddad,†‡# Chengliang Wang,†§# Haoyuan Qi,⊥ Fabian Grote,† Liaoyong Wen,† Jörg Bernhard,⊥ Ranjith Vellacheri,† Samar Tarish,†‡, Ghulam Nabi,⊥ Ute Kaiser,⊥ and Yong Lei*†

† Institute of Physics & IMN MacroNano®, Ilmenau University of Technology, Ilmenau 98693, Germany

‡ Department of Physics, College of Science, University of Al-Mustansiryah, Baghdad, Iraq

§ School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China

⊥ Central Facility of Electron Microscopy, Electron Microscopy Group of Materials Science, University of Ulm, Albert Einstein Allee 11, 89081 Ulm, Germany

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ABSTRACT: Resistive switching random access memories (RRAM) have attracted great scientific and industrial attention for next generation data storage because of their advantages of nonvolatile property, high density, low power consumption, fast writing/erasing speed, good endurance and simple and small operation system. Here, by using a template-assisted technique, we demonstrate a three-dimensional highly-ordered vertical RRAM device array with density as high as that of the nanopores of the template ($10^8$–$10^9$ cm$^{-2}$), which can also be fabricated in large area. The high crystallinity of the materials, the large contact area and the intimate semiconductor/electrode interface (3 nm interfacial layer) make the ultralow voltage operation (millivolt magnitude) and ultralow power consumption (picowatt) possible. Our procedure for fabrication of the nanodevice arrays in large area can be used for producing many other different materials and such three dimensional electronic device arrays with the capability to adjust the device densities can be extended to other applications of the next generation nanodevice technology.
INTRODUCTION

With the development of the electronic devices (e.g. tablets, cellphones, smart TV, cameras, etc.) in the market, high density and powerful data storage devices are of particular significance. There are two types of memory storage devices including volatile and nonvolatile memories.\(^1\) \(^2\) The memory storage devices such as dynamic random access memory (DRAM) and static random access memory (SRAM) which are very fast and therefore usually used as primary storage, however, are volatile and will lose data once the power supply is removed.\(^3\) \(^4\) They also suffer the waste of the peripheral circuitry and the high power consumption due to the leakage during the operation. Hence, nonvolatile memories are more desirable for long-term persistent storage, because they can store information even after the power removed or turned back on.\(^4\)

The problem is that the traditional nonvolatile memories such as magnetic random access memory (MRAM) and ferroelectric random access memory (FRAM), despite costing lower energy during the operation, they are always confined by the downscaling due to the transistor or transistor-like configuration that limits the further increasing of the device density.\(^3\) Therefore, resistive switching random access memories (RRAM) have attracted great scientific and industrial attention because they possess not only the advantages of nonvolatile property but also the high density, low power consumption, fast writing/erasing speed, good endurance and simple and small operation system.\(^3\) \(^5\) To achieve a RRAM array with high density, fast speed and low cost, the three dimensional (3D) vertical RRAM architecture (every device cell has a vertical feature to the packing plane)\(^6\) \(^7\) is particularly superior to the traditional 2D layer-by-layer RRAM cross-point array (Figure 1) in two aspects: 1) lithography process is required for every layer to pattern the features of the 2D RRAM.\(^8\) \(^9\) However, only one-time lithography is required for patterning such features in 3D vertical RRAM arrays. This advantage is even promising for
more complex devices (e.g. transistors) or further scaling down the devices (e.g. nanometer level), because of the complex, challenging and time-consuming manner of the corresponding lithography technique (e.g. electron-beam lithography).\textsuperscript{10, 11} 2) The 3D vertical RRAM array can provide high device density with larger contact (channel) area and lower sheet resistance compared with the point contact in 2D architectures.\textsuperscript{10, 12-14}

To achieve such high-density 3D resistive switching (RS) device arrays, anodic aluminum oxide (AAO) will be a good choice as a surface patterning technique. The self-organized AAO template has a high nanopore density ($10^8$–$10^{10}$ cm$^{-2}$) with adjustable nanopore size (in the range from 10 nm to 1 µm) and interspacing.\textsuperscript{15-18} The AAO membrane has been reported for RS memory arrays, as a mask to form the 2D layer-by-layer memory device array.\textsuperscript{19-21} However, the reported self-organized AAO membrane have many drawbacks, such as smaller contact area between adjacent layers, the disordering of the device array (ordered area: $< 1 \times 1$ µm$^2$),\textsuperscript{22} the absence of some lattice points, and the hexagonal nature of the nanopore arrays which makes it difficult to fabricate the device matrix.\textsuperscript{19, 23, 24} Our recent works have shown that the pre-patterned AAO membrane can form a highly-ordered square packing nanopore array over $1 \times 1$ cm$^2$.\textsuperscript{25-28} Such fabrication process also has the opportunity to produce highly-ordered nanopore arrays in wafer scale.\textsuperscript{29, 30} Moreover, the mold for the patterning can be used repeatedly and hence this one-time lithography technique is conducive to mass production and thereby further reducing the cost. These are remarkable compared with traditional lithography or other template-based techniques. In addition, the parameters (the diameter, length and the interspacing of the nanopores) can be controlled and tuned by using different imprinting mold.\textsuperscript{25}
Figure 1. Schematic diagram of the 2D layer-by-layer cross-point device array and the 3D vertical device array. Every cross-point or vertical device represents one device. The nanopores can confine the deposition of every layer in 3D architectures and thereby only one-time lithography is required for patterning the nanopores. The vertical device also possesses much larger contact area between adjacent layers.

Therefore, here, we will use AAO template to fabricate the memory device arrays for addressing the current challenge of high density RRAM. By using atomic layer deposition (ALD), we will demonstrate here that both the electrodes (TiN and Pt)\(^{26, 31}\) and semiconductor (TiO\(_2\))\(^{15}\) can be fabricated successively, forming a core-shell nanowire/nanotube array with a density of as high as \(10^8\sim10^9\) cm\(^{-2}\). Importantly, compared with the 2D layer-by-layer cross-point device arrays, the increased channel width by using the 3D nanostructures is helpful to decrease the sheet resistance and thereby to reduce the power consumption. It is important to mention that there are many kinds of materials which have been reported for RRAM, such as TiO\(_2\), ZrO\(_2\), ZnO\(_2\) and HfO\(_2\) and can be fabricated by using the similar procedure as ours.\(^{12, 32, 33}\) However, the materials are not our concerns here and therefore only TiO\(_2\) is selected as the model to demonstrate an ultralow power consumption and highly-ordered RRAM arrays with high density and repeatability, because of the advantages of TiO\(_2\) such as the easy control of its stoichiometry and crystal structure and the compatibility with traditional complementary metal-oxide semiconductor (CMOS) technology.\(^{34-36}\) This cost-effective method to fabricate such kind of 3D
electronic devices with the capability to adjust the device size and density can be extended to other applications of the next generation nanodevice technology.\textsuperscript{26}

RESULTS AND DISCUSSION

The template-assisted technique for achieving the highly-ordered 3D vertical RRAM device arrays starts from the fabrication of the AAO template. Highly-ordered porous AAO templates were prepared by using anodization of pre-patterned Al foil according to our previous work.\textsuperscript{25-27, 37, 38} The pre-patterned Al foil was obtained through imprinting of a Ni nanopillars stamp that is replicated from a silicon master mold with highly ordered nanocave arrays in a square lattice with lattice period of 400 nm. It should be noted that in this case the defect-free area was only limited by the sizes of the mold and the hydraulic pressure machine. Then the AAO template with nanopore arrays was obtained by using the anodic oxidization of the imprinted aluminum foil. In other words, the highly-ordered device arrays can be fabricated in a large area.

By choosing suitable hydraulic pressure machine and anodization cells, wafer-scale template can be expected with highly ordered nanopore arrays, providing a wafer-scale mold which can be obtained through lithography. The length of the nanopores is dependent on the anodization time and the diameter of the nanopores can be controlled by the pore-widening process. Figure 2a, b show the typical scanning electron microscopy (SEM) images of the nanopore arrays with diameter 250 and 300 nm respectively. Increasing the length of the nanopores means increasing the channel width and, therefore, reducing the sheet resistance, which is helpful to reduce the power consumption. However, the increasing of the nanopore length will hinder the miniaturization and integration of the devices. Hence, the nanopore length is controlled around 1.8 $\mu$m here. Two electrodes and the active material were deposited successively by using ALD
technique, resulting in a conductive shell of TiN nanotube, an active material TiO$_2$ nanotube array and a conducting core of Pt nanowire array.\textsuperscript{15,26,31} In this case, the core-shell nanostructure in every nanopore represents one RS device, offering a device density as high as 6×10$^8$ cm$^{-2}$. Another point worth noting is that higher device density could be expected by using a mold with lower interspacing.\textsuperscript{39} For example, a mold with interspacing of 100 nm will lead to a device density of 10$^{10}$ cm$^{-2}$.\textsuperscript{25} Even lower interspacing of 10 nm is also possible, by using suitable mold and anodic oxidization conditions, which can provide a nanopore density of 10$^{12}$ cm$^{-2}$.\textsuperscript{40} However, it should be noted that the deposition of multilayers in such small nanopores is challenging.

Figure 2c-g show the SEM images of top view of the samples after every step, corresponding to c) the AAO template, d) after deposition of TiN layer forming a TiN nanotube array (process A in Figure 2j), e) after ion-milling to remove TiN on the surface for separating every TiN nanotube electrode and thus every device (process B in Figure 2j), f) after deposition of TiO$_2$ layer giving a TiO$_2$ nanotube array located at the inner TiN nanotube (process C in Figure 2j), g) after deposition of Pt layer forming a Pt nanowire array inside of the TiO$_2$ nanotube (process D in Figure 2j). In order to show a clear image of the core-shell nanotube/nanowire arrays, ion-milling etching is used to expose the cross section of the core-shell nanostructure which consists of three materials TiN, TiO$_2$ and Pt (Figure 2h). The photographs of the samples after every deposition were shown in the supporting information (Figure S1). Through this process, the highly-ordered nanostructure array can be fabricated at the same density of the nanopores of the template in an area as large as the mold (around 1.1 cm$^2$ in this study).
**Figure 2.** Top view of SEM images of as prepared AAO template depicted the highly ordered array of nanopores with the controllable diameter of (a) 250 and (b) 300 nm ((c) magnified SEM image), respectively. SEM images of the sample (d) after deposition of TiN, (e) after surface etching, (f) after deposition of TiO$_2$, (g) after deposition of Pt, (h) after surface etching to display the core-shell nanostructure of TiN, TiO$_2$ and Pt, respectively. (i) SEM image of the backside of the sample after removing the Al and the barrier layer, showing the individual TiN nanotube shell. Scale bars of (c-i) is 500 nm. (j) Schematic outline of the fabrication processes of TiN/TiO$_2$/Pt core-shell nanotube/nanowire arrays by template-assisted ALD technique.
In order to present a clear image of the core-shell nanotube/nanowire arrays, the AAO template is removed by using phosphoric acid. Figure 3a shows a typical SEM image of the freestanding nanostructure array after removal of AAO template. Clearly, every core-shell nanotube/nanowire is one device consisting two electrodes and one active material. By using ion-milling etching, the cross-sectional view of every nanotube/nanowire is shown in Figure 3b. Such a device configuration can give a device array with density as high as the density of the nanopores ($10^8 \sim 10^9$ cm$^{-2}$). From Figure 2h and Figure 3b, it is difficult to distinguish the TiN nanotube from the TiO$_2$ nanotube, indicating that an interfacial overlap is formed between them (further proofs can be found below). Then the aluminum and alumina barrier layer at the backside were removed to expose the electrode array of TiN, as shown in Figure 2i. To protect the core-shell nanotube/nanowire array and the supportive AAO framework during the etching processes, the samples were fixed onto ITO glass with connecting ITO and Pt electrode by Ag paste. Finally, in order to demonstrate the potential application of this kind of nanostructure for RRAM application and investigate the electric performance of the device arrays by using probe station and Keithley 4200 SCS instruments, an relatively large Au film was deposited on the top surface to connect with the TiN electrode (process E in Figure 2j). It should be noted for a practical application, two cross electrode line arrays with dimension comparable to an individual nanodevice are feasible (e.g. by using electron beam lithography) and necessary to be deposited on both side of the sample for connection with TiN and Pt electrode. Such a high density of nanostructure array ($10^8 \sim 10^9$ cm$^{-2}$) makes the high density of three-dimensional (3D) vertical RRAM array possible which only needs one-time lithography for patterning the nanopores. Figure 3c shows a cross-sectional SEM image of the freestanding TiN/TiO$_2$/Pt nanostructure array, indicating a length of 1.8 µm that is coincident with the length of the nanopores. The inset
displays the energy dispersive X-ray spectrometry (EDX) line-scan profile of the cross-section nanowire arrays. From the EDX spectra, it is clear that a core-shell nanostructure was obtained, consisting a TiN nanotube shell, a Pt nanowire core and a TiO$_2$ nanotube between them. The EDX line-scan profile (Figure S2) of a single core-shell nanostructure clearly confirms the formation of the desired materials and the thickness of TiN, TiO$_2$ and Pt are 30, 70 and 28 nm (diameter of Pt nanowire is about 55 nm) respectively.\textsuperscript{15, 26, 31} Furthermore, the EDX profile of TiN/TiO$_2$/Pt nanotube/nanowire emphasize the high purity of elements (Figure S3). Figure 3d shows the X-ray diffraction (XRD) pattern of the as-prepared core-shell nanostructure arrays. The TiN nanotube can be identified to osbornite phase and the main diffraction peaks at 36.6°, 42.5° and 61.8° can be indexed to (111), (200) and (222) orientations, respectively. The TiO$_2$ nanotube belongs to anatase phase and the highest intensity diffraction peak at 25.3° can be indexed to face (101). The highest intensity diffraction peak of Pt nanowire was oriented at 39.4°, which can be assigned to face (111) of the Pt. The high intensities of the XRD patterns suggest that the three materials are highly crystalline.
**Figure 3.** (a-b) Top view SEM images of core-shell nanotube/nanowire array of TiN/TiO$_2$/Pt: (a) freestanding and (b) after etching to display the core-shell nanostructures without removal of the template. (c) Cross-sectional SEM images of freestanding core-shell nanotube/nanowire array of TiN/TiO$_2$/Pt with inset of EDX line-scan profile. (d) XRD patterns of TiN/TiO$_2$/Pt core-shell nanotube/nanowire arrays with standard XRD patterns of each component from Crystallography Open Database (COD).

The composition and the structural information of the core-shell nanostructure were further examined by transmission electron microscopy (TEM). The TEM lamella was prepared by using focused ion beam equipment (the detailed fabrication process can be found in Figure S4, S5 and S6). Figure 4a shows a cross-section TEM image of one individual core-shell nanotube/nanowire, which consists of three materials inside of the nanopores of the highly ordered AAO template. The intensity profile across the nanostructures in the inset of Figure 4a indicates that the thicknesses of TiN, TiO$_2$ and Pt layers were 30, 70 and 28 nm, respectively, which is coincident with the EDX measurement in Figure S2. It should be noted that the surface of every layer is very smooth, which is indisputable for the conformal deposition of ALD and can be observed in the cross-sectional SEM images (Figure 2 and 3). Figure 4b-c presents the high resolution transmission electron microscopy (HRTEM) images of the two interfacial areas of TiN/TiO$_2$ (the area I in Figure 4a) and TiO$_2$/Pt (area II in Figure 4a). The HRTEM images indicate that the three materials are highly crystalline with clear crystal lattice fringes. The HRTEM images further proved that the components of the three areas are TiN, TiO$_2$ and Pt respectively. The facet distance of area III is 2.44 Å, which can be indexed to the TiN (111) facet with an interplanar spacing of 2.49 Å by using the crystal structure of refcode 1011099 from the
COD. The facet distance of area IV is 3.53 Å, belonging to the TiO$_2$ (101) facet that has an interplanar spacing of 3.52 Å by using the crystal structure of TiO$_2$ (refcode 7206075 from the COD). On the other hand, area V has a facet distance of 2.26 Å, which is close to the interplanar spacing of Pt (111) facet (2.27 Å, refcode 9008480 from the COD). Moreover, a clear interfacial layer was observed at the interface between TiN and TiO$_2$. This interfacial layer probably was generated from the surface of TiN due to the exposure to oxygen for the deposition of TiO$_2$.

![Figure 4](image)

**Figure 4.** (a) Cross-sectional TEM images of one individual nanostructure containing an Al$_2$O$_3$ nanopore, a TiN nanotube, a TiO$_2$ nanotube and a Pt nanowire. HRTEM images of (b) area I showing the interface between TiN and TiO$_2$, and (c) area II showing the interface between TiO$_2$ and Pt.

Figure 5a, b present the magnified HRTEM images of the interfacial area (the area I in Figure 4a) between TiN and TiO$_2$, where the overlapping of the crystal lattice fringes of TiN and TiO$_2$ can be clearly observed. The overlapping interfacial layer is as large as 3 nm. The FFT pattern and the inverse FFT images support the formation of the thick interfacial layer between TiN and TiO$_2$. 
the TiN electrode and TiO$_2$ (Figure S7). Such interface is expected to enhance the interfacial 
compatibility and reduce the defects and resistance (potential barrier, contact resistance) between 
the electrode and the semiconductor, therefore, facilitate the charge transport between them.$^{42,43}$

![HRTEM images of the interface between TiN and TiO$_2$.](image)

**Figure 5.** (a, b) HRTEM images of the interface between TiN and TiO$_2$.

Figure 6 shows an asymmetrical I-V curves (semilogarithmic) based on the TiN/TiO$_2$/Pt 
nanostructure array (diameter of the nanopores is about 250 nm for S1 and 300 nm for S2), 
indicating a sharp increase of the current around the potential of -1.5 and -1.4 mV in reverse bias 
(or +1.2 and +1.1 mV for forward), respectively. The asymmetrical property can be ascribed to 
the asymmetrical device configuration. Normally, it is believed that the bipolar resistive 
switching behavior is due to the migration of oxygen ions.$^{44-46}$ When a positive electrical field is 
applied to the TiN electrode, the oxygen ions, generated from the interfacial area between TiN 
and TiO$_2$ due to the injection of the electrons, will be drawn to the TiN electrode, resulting in an 
oxygen reservoir in the TiN electrode and leaving oxygen vacancies in the conducting channel. If 
the electric potential (set potential) is higher than the threshold potential, the device switches into 
the low resistance state (LRS) from the high resistance state (HRS). On the contrary, if a reverse 
bias (reset potential) is applied on TiN electrode, the oxygen ions are pushed from the TiN 
electrode and fill in the oxygen vacancies in the conducting channel, leading to a high resistance
state afterward. Because the oxygen ions fundamentally existed in the TiN/TiO$_2$ interface and oxygen reservoir was not observed in the Pt/TiO$_2$ interface (also see Figure 4), the set potential (+1.2 or +1.1 mV) is lower than the reset potential (-1.5 or -1.4 mV). Normally, the reported threshold potential is higher than 0.2 V obtained from thin film device or 2D layer-by-layer cross-point device array. However, our results are reproducible. Tens of devices were studied and all of them showed similar switching properties even after hundred cycles (Figure 7).

Such low threshold potential probably can be attributed to the large contact area of the 3D vertical device array, the high crystallinity of the semiconductor and the electrodes, the low defect density as well as the intimate interface between the TiN electrode and the TiO$_2$ active material (Figure 4 and 5). Both millivolt-scaled threshold potential are amazing which makes it possible to apply the core-shell nanostructures for ultralow power consumption RRAM (several pW). The device formed a complete switching cycle when scanning back, indicating the reversible electrical bistable switching property of the nanostructures.

Figure 6. Semilogarithmic I–V characteristics as a comparing of RS behavior of two different diameters of TiN/TiO$_2$/Pt core-shell nanotube/nanowire. The insets are a schematic description of the oxygen ion (blue point) and vacancy (white point) distribution inside TiO$_2$. The polarity of the applied voltage during each stage represented by + and -.
As mentioned above, compared with the nanodot arrays, the increased channel width by using the 3D nanostructures is helpful to decrease the sheet resistance and thereby to reduce the power consumption. It is clear that besides of the material itself, its morphology and structural packing, the channel length and width also affect the sheet resistance. In order to verify our assumption, here two kinds of samples with a different diameter of the nanopores (same length of the nanopores and the same thickness of the active materials), i.e. having different channel width or contact (channel) area, were investigated, shown in Figure 6. The contact area of sample with diameter of 300 nm increases by 20% relative to the one with diameter of 250 nm. As expected, the threshold potential shifts slightly from -1.5 (or +1.2) mV to -1.4 (or +1.1) mV respectively, suggesting the effect of the contact area (or the sheet resistance) on the power consumption. 30 devices were examined for each diameters. All these results indicate that the ultralow power consumption is due to the high crystal quality of the materials, the low defect density, the large contact (channel) area, the intimate interface between the semiconductor and the electrodes and the suitable device configuration.

Figure 7a, b show 300 cycles of bipolar resistive switching properties of two different samples with diameter around 250 nm and 300 nm, respectively. Both the HRS and LRS are very stable, indicating the excellent electrical stability of the core-shell nanostructures. Both the two samples show high repeatability of the switching behavior even after 300 cycles. The high electrical stability for both low resistance state (LRS) and high resistance state (HRS) at 0.3 mV are shown in Figure 7c, which are extracted from the results in Fig. 7a-b. There is no significant variation even after cycled 300 times. In order to demonstrate the potential application of these high density core-shell nanostructures for memory device, writing-reading-erasing-reading cycles were applied onto the device. As shown in Figure 7d, the almost simultaneous response of
the current to the writing and erasing process and the high on/off ratio (LRS/HRS resistance ratio) indicate its capability for high-speed memory applications. Moreover, the switching process from OFF state to ON state is reproducible without any obvious variation, which confirms the stability of switching behavior.

**Figure 7.** (a, b) Typical I–V curves (300 cycles) of single TiN/TiO$_2$/Pt core-shell nanostructure with the diameter of 250 and 300 nm, respectively. The inset shows the low threshold potential of SET and ReSET stages. (c) Endurance performance (3000 cycles) of TiN/TiO$_2$/Pt core-shell nanostructure, showing the high stability for both HRS and LRS. (d) Writing-reading-erasing-reading cycles of TiN/TiO$_2$/Pt memory device. The writing, reading, erasing and reading potentials are 2.0, 0.3, -2.0 and 0.3 mV respectively.
CONCLUSIONS

In summary, a core-shell nanowire/nanotube array with a density of as high as $10^8$~$10^9$ cm$^{-2}$ was fabricated by using a template-assisted technique. Even higher density (e.g. $10^{12}$ cm$^{-2}$) can be achieved by using lower interspacing (10 nm), although the deposition of multilayers in such small nanopores is challenging. We demonstrated that both the electrodes (TiN and Pt) and semiconductor (TiO$_2$) could be fabricated by using conformal ALD technique. The potential application of this core-shell nanostructure array for RRAM was presented. Such 3D vertical RRAM array can provide high device density with the same density of the nanostructures which only needs one-time lithography for patterning the nanopores and hence is superior to 2D architectures (multi-time lithography) and traditional lithography (unfavorable for mass production). Because of the high crystallinity of the materials, the large contact area and the intimate interface (3 nm) between the TiN and TiO$_2$, ultralow voltage operation (mV magnitude) and ultralow power consumption (pW magnitude) were achieved. It should be noted that many kinds of materials can be fabricated by using the similar procedure with ours. The materials used here are to demonstrate the template-assisted technique for creating a non-volatile memory technology as proof of concept. This cost-effective method to fabricate such kind of 3D electronic device arrays with CMOS-compatibility and the capability to adjust the device densities can be extended to other applications of the next generation nanodevice technology.

EXPERIMENTAL SECTION

Preparation of AAO templates. Highly ordered AAO templates with different diameters were prepared by using high-purity (99.99%) aluminum foil with a thickness of 0.2 mm according to
our previous reports. Al foils were first cleaned by acetone, ethanol and DI water successively then electrochemical polished in a 1:7 solution of perchloric acid and ethanol. The Ni stamp with nanopillar periods of 400 nm was placed on electropolished Al foil, and a reverse replication of nanopillar array was conducted on the Al foil by using an oil press under a pressure of about 10.0 MP for 10 min. The anodization of the Al foil was performed under a constant voltage of 160 V in 0.4 M H$_3$PO$_4$ at 15 °C for 10 min. The obtained AAO templates were put in 5 wt % of the H$_3$PO$_4$ solution at 30 °C to realize desirable pore-diameter. After 120 or 140 min of the pore-widening process, the resulted AAO template will have a pore diameter of about 250 nm and 300 nm, respectively.

**Fabrication of the core-shell nanostructure arrays.** The deposition of TiN/TiO$_2$/Pt core-shell nanostructure arrays was conducted in a Picosun SUNALETM R150 ALD System. The AAO template was placed in the chamber of the ALD system and TiN was first deposited at a temperature of 400 °C. TiCl$_4$ and NH$_3$ were used as precursors with respective pulse/purge times of 0.1 s/6 s and 1 s/10 s and a carrier gas flow of 120 sccm. N$_2$ gas was used as both carrier and purge gas. This ALD process was repeated 1700 times, leading to TiN layer of about 30 nm. Before the deposition of the TiO$_2$, the surface of the sample was etched by ion-milling with an angle of 60° at energy power of 5 kV and rotation of 5 Hz to remove the top surface of TiN, leading to separated TiN nanotube arrays for achieving high density device arrays. To deposit the second layer of TiO$_2$, two-step ALD procedure was adopted to deposit 1200 cycles of TiO$_2$ layer by using TiCl$_4$ and H$_2$O as Ti and O sources under 25 °C.$^{15}$ The typical pulse/purge time for TiCl$_4$ and H$_2$O precursors was 0.1 s/5 s and the carrier gas flow was set at 200 sccm. The first step of TiO$_2$ deposition was carried out at 250 °C for 40 cycles (1.84 nm) forming a continuous TiO$_2$ layer. Then the sample was annealed (inside the ALD chamber) at 480 °C for 1 h to create a
highly crystalline seed layer for the next 1160 cycles of TiO$_2$ deposition at 400 °C. Then Pt was deposited as the other electrode under a chamber temperature of 300 °C and a Pt(MeCp)Me$_3$ precursor temperature of 80 °C. 500 ALD process cycles were conducted for the deposition of Pt nanowire array with typical pulse/purge time of Pt(MeCp)Me$_3$ and O$_2$ was 1.3 s/30 s, while the N$_2$ carrying gases are kept at 100 sccm.

**Device fabrication and characterization.** After the fabrication of the core-shell nanostructure arrays, the Al on the backside of the AAO template was removed in a mixture solution of CuCl$_2$ (90 wt %) and HCl (10 wt %). The sample was transferred in 5 wt % H$_3$PO$_4$ solution at 30 °C for 50 min to remove the alumina barrier layer (formed during the oxidization) and show up the TiN nanotube electrodes. Using a line array shadow mask with distance $3 \mu$m, Au thin film (30 nm) was deposited by using electron beam physical vapor deposition from Kurt J. Lesker. The SEM images and EDX patterns of the as-prepared core-shell TiN/TiO$_2$/Pt nanostructure arrays were investigated using a scanning electron microscope (SEM, Hitachi S4800). HRTEM images were performed on an image-side Cs-corrected FEI Titan 80–300 microscope operated at an acceleration voltage of 300 kV. X-ray diffraction patterns were studied by utilizing a Siemens D5000 XRD equipment. Electrical measurements of the fabricated devices were performed using a micromanipulator 4060 probe station connected to a Keithley 4200-SCS semiconductor characterization system with pre-Amplifier in the air atmosphere.

**Supporting Information.** Photographs of the depositions steps, EDX line-scan profile of the single nanotube/nanowire, cross section TEM lamella preparation, analyzing the HRTEM of the interfacial layer between TiN and TiO$_2$. This material is available free of charge via the Internet at http://pubs.acs.org.
Corresponding Author

E-mail: yong.lei@tu-ilmenau.de

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. # These authors contributed equally.

Conflict of Interest: The authors declare no competing financial interest.

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