Characterization of Strain-Compensated 980 nm Bottom-Emitting VCSELs

Ihab Kardosh, Michael Riedl, and Fernando Rinaldi

A new design of strain-compensated 980 nm bottom-emitting VCSELs is presented. Single devices and specially designed 3 × 3 VCSEL arrays have been successfully fabricated and characterized.

1. Introduction

Laser devices emitting in the 980 nm spectral region are interesting for many applications like pumping of solid-state lasers, pumping of optical amplifiers and frequency doubling for visible laser light generation. VCSELs with high output power and a good beam quality are attractive for such applications. In this work, strain compensation using phosphorus-containing layers close to the active region has been introduced for the first time, resulting in a considerable reduction of output power degradation and thus in an increase of the laser lifetime. Single laser devices have been fabricated and characterized on wafer, whereas laser arrays consisting of 9 devices have been mounted on heat sinks for simultaneous laser operation and for sufficient heat removal.

2. Device Fabrication

Figure 1 shows a schematic drawing of a typical bottom-emitting VCSEL. The sample consists of InGaAs quantum wells separated by GaAs barrier layers. GaAsP layers are introduced close to the active region for strain compensation. An AlAs layer in the p-side region is required for current confinement. After mesa etching, selective oxidation of the AlAs layer is performed to define the current aperture. Metallization layers are then evaporated to form a circular p-type contact on top of the mesa. Before mounting the devices on heat sinks, the substrate is usually thinned to reduce absorption and to ease cleaving. A Si_3N_4 anti-reflection (AR) coating is then deposited in the opening of the n-type contact on the substrate side.

2.1 VCSEL arrays

The fabricated VCSEL arrays consist of 3 × 3 devices each with an active diameter of 30 µm. Before mounting the devices upside down on heat sinks, a passivation layer of Si_3N_4 is deposited around the p-contacts to avoid any short circuits on mesa edges during the soldering process. Figure 2 shows two photographs of a laser array. The p-type

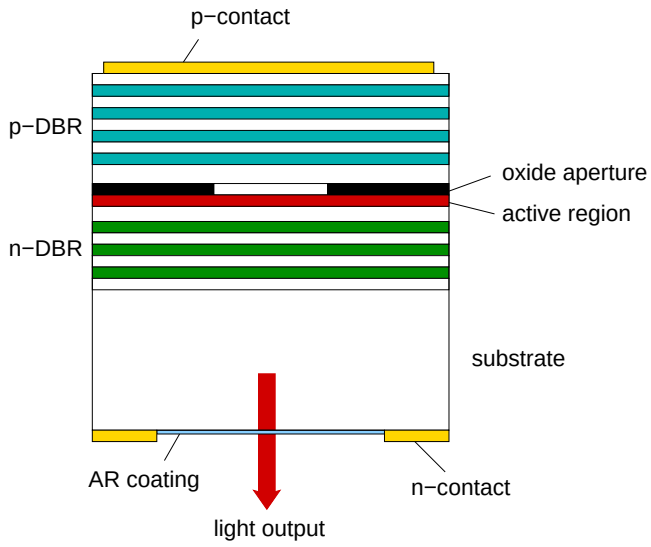

Fig. 1: Schematic cross-section of a bottom-emitting VCSEL.

metallization contacts and the silicon nitride passivation layer can be seen on the left. The substrate side with the n-type metallization is shown on the right. The chip area of about $1.25 \times 1.25\,\mathrm{mm}^2$ is indicated by the dashed lines. Individual chips containing VCSELs placed at 500 µm pitch are separated by cleaving.

The 3×3 VCSEL module is shown in Fig. 3. A cleaved chip is soldered epitaxial side down with indium to a copper heat sink. An underfill is used for mechanical stability. Gold wires are bonded from the electro-plated gold on the substrate side to the $(-)$ connector. The copper holder serves as the $(+)$ connector.

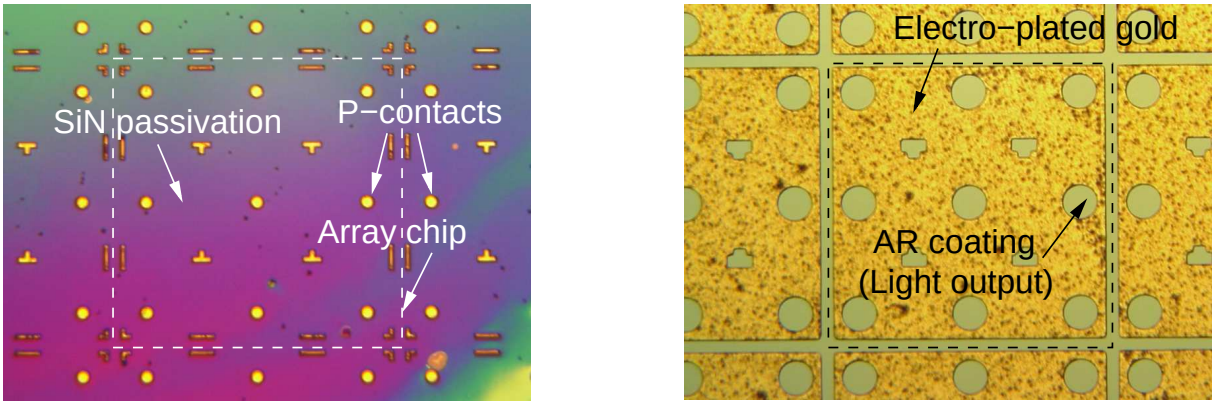

Fig. 2: Photographs of the epitaxial side (left) and the substrate side (right) taken after processing of the 3×3 VCSEL array.

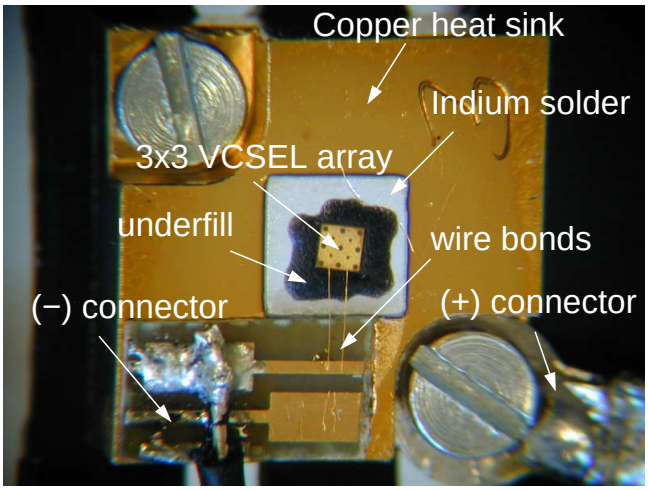

Fig. 3: Laser module containing the 3×3 VCSEL array. The array chip is soldered with indium to the gold-plated copper heat sink.

3. Characterization

VCSELs with different active diameters have been measured on wafer. In general, in addition to the lifetime improvement, the devices show a higher output power and differential quantum efficiency than standard bottom-emitting VCSELs without strain compensation [1]. In Fig. 4 the light–current–voltage (LIV) chracteristics of VCSELs with two different active diameter D_a can be seen. Extracted data like threshold current I_th, maximum output power P_max, differential quantum efficiency η_d, maximum wall-plug efficiency $\eta_\mathrm{wp,max}$, and emission wavelength λ are listed in Table 1.

Table 1: Key parameters of the devices from Fig. 4.

D_a [µm]	I_th [mA]	P_max [mW]	η_d [%]	$\eta_\mathrm{wp,max}$ [%]	λ [nm]
14	1.6	21.8	63	24.7	965
25	3.7	32.4	62	21.9	967

3.1 3×3 VCSEL array

The LIV characteristics of the VCSEL array module are displayed in Fig. 5. The devices have an individual oxide aperture of about 30 µm diameter. Key array data are 145 mA threshold current, 45 % differential quantum efficiency, and an output power of about 400 mW at 720 mA driving current. The IV curve shows 1.9 V threshold voltage and about 3 Ω average differential resistance. The module emits in a wide spectral range of about 10 nm at a driving current of 620 mA.

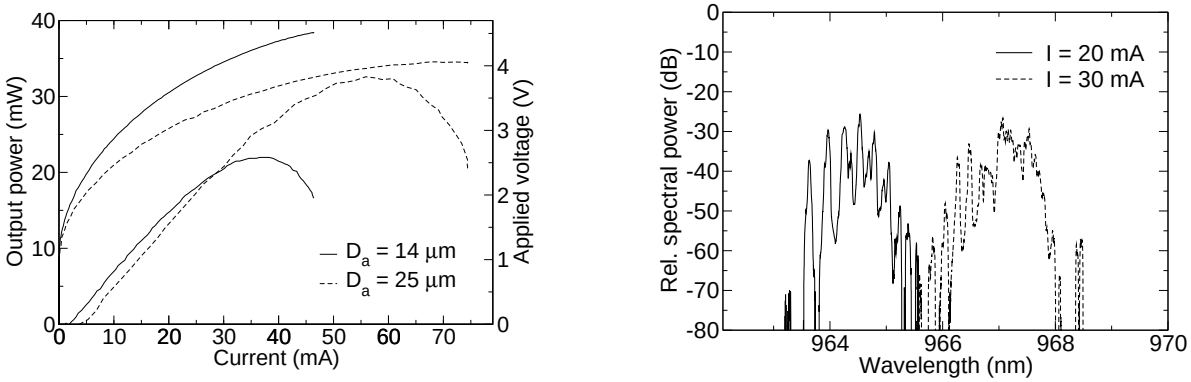

Fig. 4: LIV characteristics (left) and spectra (right) of bottom-emitting VCSELs with 14 µm and 25 µm active diameters.

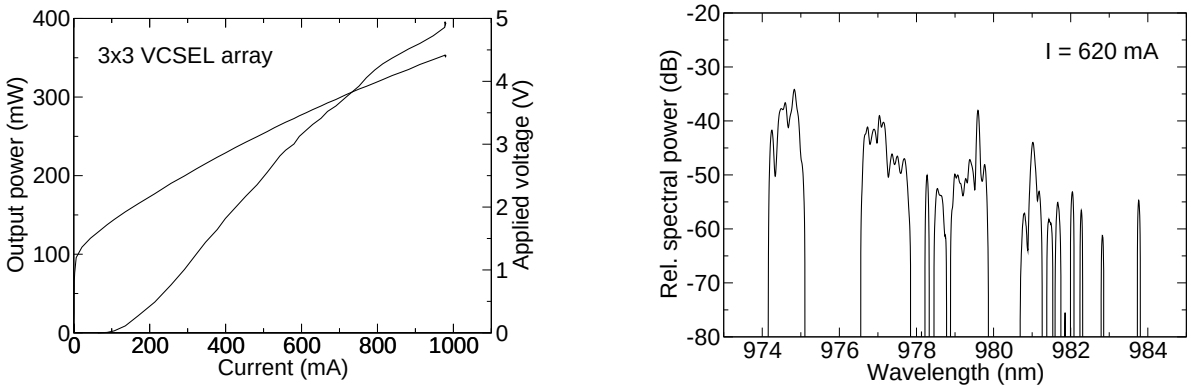

Fig. 5: Operating characteristics of the 3×3 VCSEL module from Fig. 3.

4. Conclusion

In this work, bottom-emitting VCSELs have been fabricated and characterized. A new layer design using GaAsP layers close to the active region has been implemented. In comparison with standard bottom-emitting VCSELs, the strain-compensated devices show higher output power and an increase in differential quantum efficiency. VCSEL arrays consisting of 3×3 elements have been also fabricated and characterized. The custom-designed arrays have a chip area of $1.25 \times 1.25\,\mathrm{mm}^2$ and a device pitch of 500 µm. An output power of about 400 mW is achieved from devices with 30 µm active diameter.

References

[1] I. Kardosh and F. Rinaldi, "Fabrication and characterization of 980 nm bottom-emitting VCSELs", *Annual Report 2005,* pp. 45–48. Ulm University, Institute of Optoelectronics.