

Sample Support Development for In-Situ Ultra-HRTEM Electrical Investigations

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Specially designed sample supports have been developed to permit in-situ investigation of the electrical conductivity of ultrathin samples e.g. sheets of graphene or semiconductor nanofoils in a high-resolution transmission electron microscope (HRTEM). This report describes different ways of realization of a suitable sample platform including the corresponding electrode support geometry.

1. Introduction

The measurement of the influence of adsorbates in terms of individual molecules or atoms on the conductivity of ultrathin materials at simultaneous visualization of events taking place on atomic scale opens not only new horizons in basic research but also provides a well-founded scientific background with regard to potential sensor applications as proposed by F. Schedin et al. [1] in 2007.

In principle the performance of (in-situ) electrical studies in a HRTEM offers a very attractive solution. On one hand, it provides an effective real-time observation of the sample; on the other hand — at adequately low acceleration voltages — it is a relatively non-destructive characterization method for a wide range of materials.

In order to achieve this goal, the respective samples should be both simultaneously: eminently thin and free-standing. With respect to this technological challenge, world wide only few successful experiments are known. In case of semiconductor nanofoils so far no experiments are known. In case of graphene there is one, but very elaborate measuring principle. On this, a sheet of graphene is mounted on a standard TEM grid to realize an electrode from the samples backside. The second contact is made by a scanning tunneling microscope (STM) tip using a particular TEM–STM platform [2, 3].

Here, we present various approaches to realize an in situ electrical measuring sample platform. These sample supports are not only uniquely adaptive but also provide reproducible environmental conditions, which is one of the most important aspects to gain quantitative information and in the face of future applications.

2. Fabrication Approaches

2.1 Approach I: Procedures based on commercially available and already perforated SiN membranes

Commercially available support chips on the basis of silicon with a maximum diameter of 3.05 mm are already very common for TEM investigations. In general they consist of

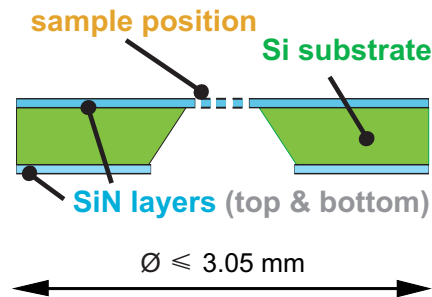


Fig. 1: Schematic cross-sectional view of a typical TEM sample support chip.

two insulating nitride (SiN) or dioxide (SiO₂) layers. One is located at the upper and a second one at the lower surface of a silicon substrate. To achieve a perforated membrane, each of these films needs to be structured. Into the top layer, arrays of little opening are etched on which the sample later will be positioned. The masking of the bottom layer is used to etch selectively large areas of exposed silicon up to the opposing top layer (Fig. 1). The thickness of the resulting SiN or SiO₂ membrane, hole diameter as well as hole pitch are typical size parameters offered for sale to choose them according to the individual requirements (Fig. 2).

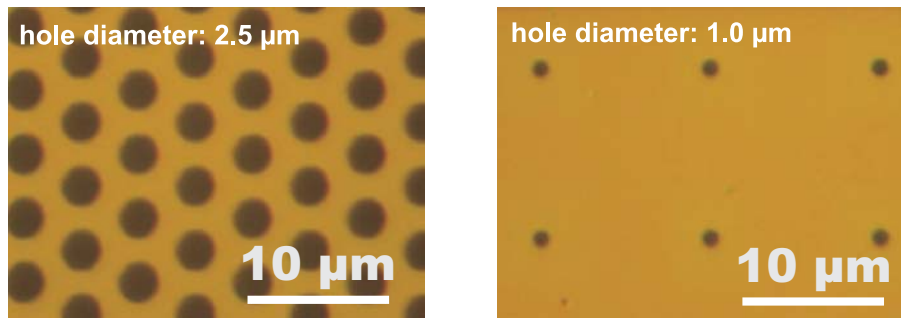


Fig. 2: Two optical micrographs of purchasable SiN membranes with different hole maskings.

Optical lithography is usually the most efficient way to deposit metal electrode structures on these membranes. In this context one should check if the sample supports offered by the supplier are only available as single frame chips or in terms of single frames joint with each other to a so called multi frame array (Fig. 3 a). In the latter case, annoying side wall formations arising from the photo resist can be easier avoided. Otherwise edge beads near the membrane will not only cause loss in lithographic resolution but also reduce dramatically the surface effectively usable for lithographic applications (Fig. 3 b).

Furthermore, after exceeding a critical hole pitch and diameter, resist ripples can arise along the perforated membrane areas leading again to losses of the lithographic resolution (Fig. 3 c). The magnitude of these parameters depends on the viscosity of the photoresist and the occurring surface tension.

Moreover, prior to each resist coating an oxygen plasma treatment of the chip surface is highly recommend. Otherwise the implied surface tension can tend to a rolling off of the liquid during the spin coating process (Fig. 3 d,e).

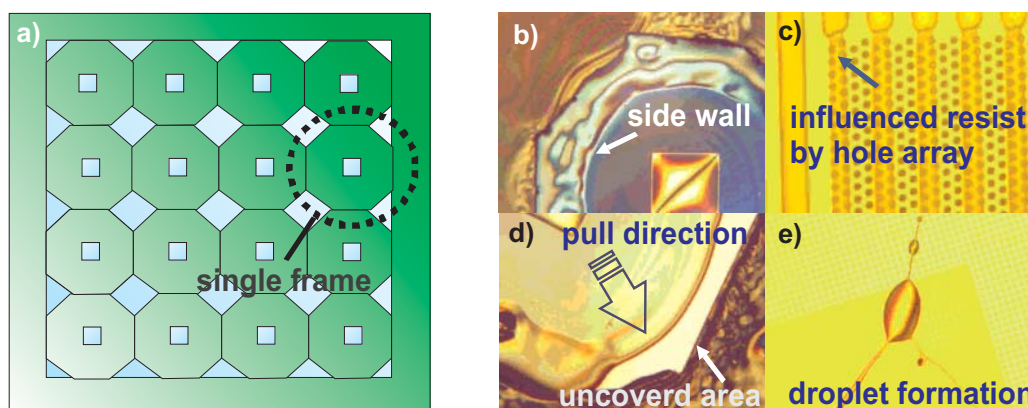


Fig. 3: a) Schematic illustration of a multi frame array chip. This arrangement allows the simultaneous processing of several single frames which can be snapped out, when all lithographic steps are finished. b) Optical micrograph of a single frame chip coated with resist exhibiting highly distinct side wall formations on its edges. c) Resist stripes covering a SiN membrane, where the homogeneity of the thickness is strongly influenced by the perforation. d) Corner region of a single frame chip: Here, the resist tended to a droplet formation. Uncoated areas are remaining, because only a little droplet became pulled apart from the center towards the sample edges. The most of the resist got slipped away during the spin coating by the centrifugal force. e) After the coating only few resist droplets are still adhering at the SiN surface - almost all of the resist got slipped away.

For simple two probe measurements, an interdigitated finger electrode geometry is recommended. This is at most flexible with regard to the sample position (Fig. 4).

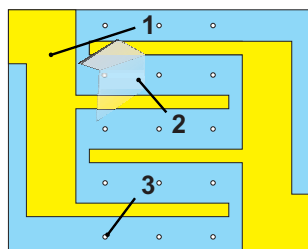


Fig. 4: Schematic top view how an interdigitated finger electrode structure could be easily realized: 1) Metal electrode structure. 2) The sample material e.g. a flake of graphene. 3) In-between the electrodes located membrane holes, onto which the sample should be positioned.

2.2 Approach II: Procedures based on commercially available and non-perforated SiN membranes

In order to gain more flexibility concerning sample size and electrode geometry, in this approach the membrane hole parameter are chosen by oneself. This can easily be achieved by a focused ion beam (FIB) etching procedure (Fig. 5). For this purpose we use the same commercially available TEM support chips, just without perforation of the SiN membrane.

This approach takes advantage if the sample can be positioned accurately, not only in terms of the electrode and hole design. Also a smaller amount of holes and likewise smaller sizes of the SiN membranes can be chosen to improve its mechanical stability. This of particular importance in view of lithography based processes, e.g. electrode fabrication as described above.

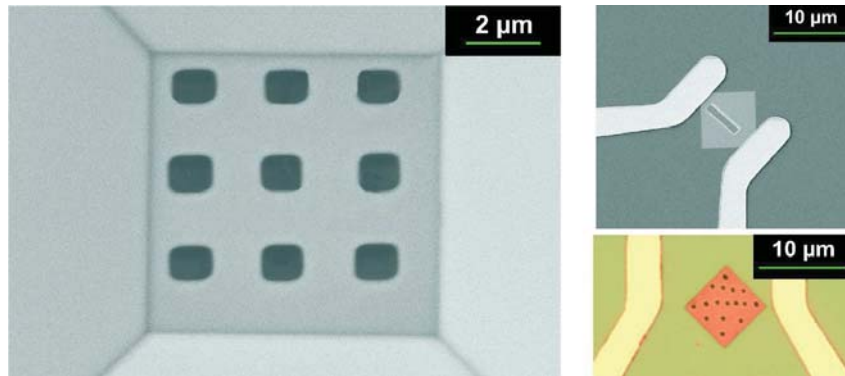


Fig. 5: Scanning electron microscope (SEM) view of variously FIB-perforated membranes from the back (left) and top side (right). Gold electrodes were deposited beside the FIB-fabricated openings.

2.3 Approach III: Procedures based on self-fabricated SiN membranes

Opposite to the approaches described before, the following procedure is based on self-fabricated support chips. Thereby one gains a maximum of flexibility with regard to the choice of electrode or membrane hole design as well as simplified handling during its lithography based fabrication processes.

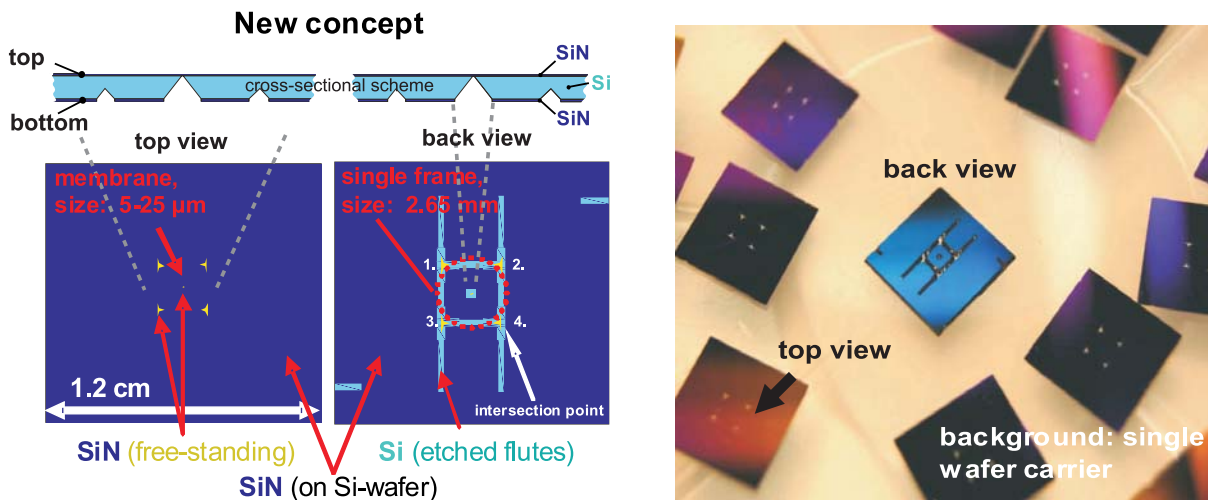


Fig. 6: Left: Drawing of the top and back view of the advanced single frame chip design including a scheme of its cross-sectional area. Right: A photograph of self-fabricated support chips exhibiting specified SiN membrane sizes of around 25 μm.

Similar as for the commercially available chips, the free-standing SiN areas are achieved by using highly anisotropic wet-chemical etching (KOH solution) of unmasked (100) Si surfaces. Simultaneously etched flutes — which include automatically achieved freestanding SiN “triangles” at the four intersection points (numbered in Fig. 6) — enable simple cleaving to remove the surrounding chip areas from the central single frame after sample preparation is finished.

Large, unstructured chip areas around the single frame provide optimum conditions for

resist coating in terms of lithographic applications and the avoidance of accidental cracking into several single or double-frame chips upon contact with a lithography mask or removal of the sample from conductive carbon pads, which are typically used for SEM/FIB sample mounting.

A similarly important benefit of the mechanically stable surrounding areas is the possibility of etching marker structures into the SiN layer to enable the precise sample alignment that is required for subsequent e-beam-writing processes.

After the support chip fabrication itself, electrode structures were deposited onto the SiN membrane (Fig. 7, left). The metal layer system consists of 10 nm titanium, 30 nm gold and again of approximately 100 nm titanium. The top layer is used to protect the gold layer from a tetrafluoromethane plasma introduced by the reactive-ion etching (RIE) machine. Latter is needed to realize precisely a vertical slit in-between the electrodes, in terms of using the electrode structure itself as mask (self-alignment). After the dry etching process the upper titanium layer becomes selectively removed, together with a temporary photoresist mask used to protect the exposed SiN surface around the electrodes (Fig. 7, right).

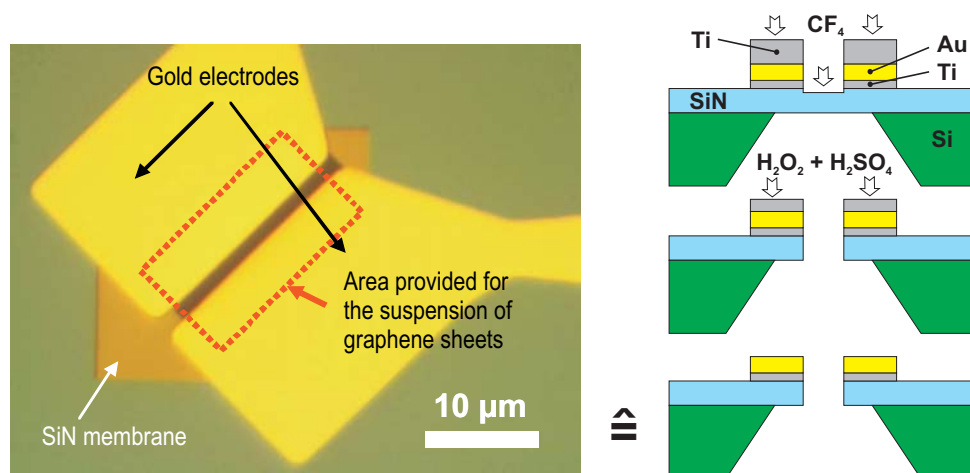


Fig. 7: Left: Optical micrograph of an advanced support geometry. Right: Schematic illustration of the layer system and fabrication steps to achieve such an electrode support structure

The main advantage of this electrode design is that the sample is actually suspended only between the two electrodes and not interacting with any support material. In other words we achieved optimum conditions to perform highly sensitive electrical measurements, especially with regard to the influence of adsorbate-induced surface states on conductivity.

3. Conclusion

We introduced three different approaches to fabricate in a most efficient way and according to individual demands a sample platform which is fully capable to perform in situ electrical measurements on a HRTEM. The first two methods are based on commercially available TEM support chips and hence they represent the cheapest and fastest way. The third

and most promising possibility is an alternative to gain the optimum of flexibility with respect to the further processing and possible applications.

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