VCSELs With X-Shaped Cavity: Cool and Fast

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We present a novel type of AlGaAs/GaAs-based vertical-cavity surface-emitting laser (VCSEL) and two-dimensional arrays with an X-shaped cavity cross-section which we term XCSEL. The devices are cool in the sense that they have record-low thermal resistances after flip-chip bonding and substrate removal, which will allow high-density hybrid integration with electronic circuitry in future optical interconnects. Common approaches for efficient heat removal increase the parasitic laser capacitance and limit the operation speed. This effect is minimized in the new devices — they also remain fast.

1. Introduction

VCSELs are firmly established coherent light sources in optical sensing and data communications [1]. The overwhelming majority of commercial devices is based on GaAs quantum well (QW) technology for emission wavelengths in the 840–860 nm spectral window. This holds for both position sensors like optical computer mice and optical interconnects over multimode fiber (MMF). The latter topical area has gained much momentum in recent years. All major VCSEL companies are intensively working on next-generation higher-speed devices to keep up with the growth predicted in roadmaps of, e.g., the InfiniBand or Fibre Channel standards. Data rates of 25 to 28 Gbit/s data rates are the next step for commercial VCSELs.

In order to be a viable alternative to electrical lines, a higher channel count of optical intra-system links is needed over shorter and shorter distances [2]. Simultaneously there is a strong need for cost reduction. Moreover, compared to established data communications transceivers, a transmitter formed by the hybrid integration of VCSELs with electronic circuits will experience higher ambient temperatures which are known to reduce laser reliability in an exponential way [3]. Hence, for such systems, high-speed VCSEL arrays are sought which can be manufactured at lower cost, can be integrated with electronics, and show reduced self-heating. We attempt to take a step in this direction by proposing a novel type of 850 nm VCSEL and two-dimensional (2-D) array that provide such benefits without obvious drawbacks for their dynamic performance.

We will briefly introduce the novel device concept and the fabrication approach. Thermal properties of manufactured prototype lasers as well as their static and dynamic characteristics are then presented.

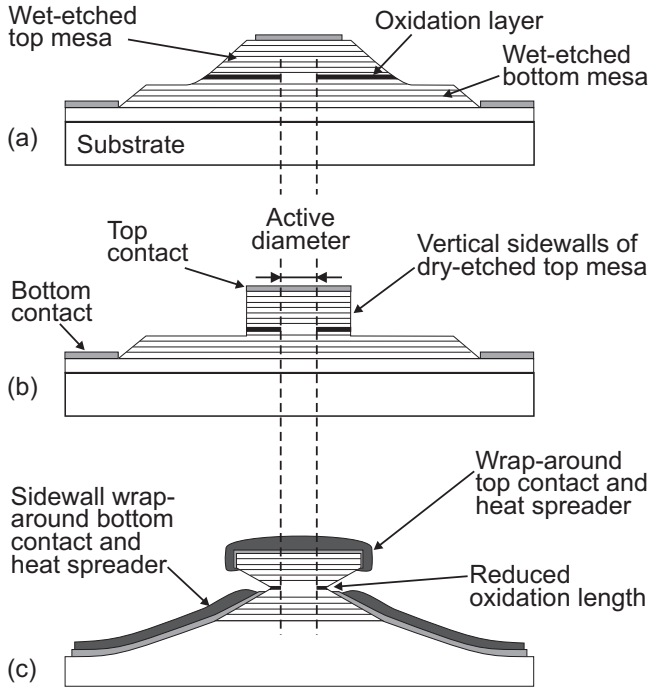

Fig. 1: (a) Conventional wet-etched VCSELs. (b) Conventional dry-etched VCSELs with vertical top mesa sidewalls. (c) XCSEL exhibiting the characteristic X-shaped outline.

2. Device Concept

The basic idea behind the new scheme is both simple and effective: instead of eliminating the influence of the sidewalls, they are utilized in a new way with benefits for both the fabrication as well as the performance of the lasers. It is not attempted to alleviate surface topography to apply planar technology but useful three-dimensional profiles are shaped in the wafer surface. This involves a novel shape forming of VCSEL sidewalls using a generic etch process by simply exploiting etch rate differentials between layers of different material compositions. In a simple case, this may produce vertical sidewalls with one circumferential geometric constriction as in an hourglass.

Part (c) of Fig. 1 shows an exemplary schematic cross-section of such a device in comparison to conventional wet-etched (part (a), see also [4]) and dry-etched (part (b), see also [5]) VCSELs. In conventional wet-etched VCSELs, tolerances for manual contact lithography impede further miniaturization. Large and poorly defined oxide widths lead to deviations of active diameters, parasitic capacitance, and blockages to heat flow. There is moreover no possibility to integrate efficient cooling structures. The vertical mesa sidewalls in part (b) are obtained by relatively expensive dry-etching techniques that somewhat reduce the oxide width and ensure a better reproducibility of the active diameters. The new device in part (c) has both optimized properties and requires substantially fewer processing steps. The notch in the center has consequences for the 1) guiding of the optical field in the laser, 2) current injection, 3) heat extraction from the core of the device, and 4) overall strategy of fabrication. By giving the sidewalls a structure that includes notches or constrictions with sections of negative sidewall angle, it becomes possible for the first time to truly control a structured metal deposition in the vertical dimension with sub-micrometer precision. As a consequence, integrated cooling structures compatible with high-frequency modulation are possible.

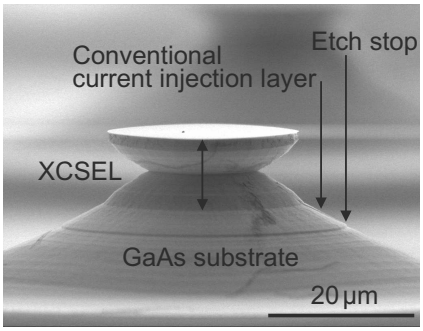

Fig. 2: SEM image of a typical XCSEL with a small sidewall constriction.

Figure 2 shows a scanning electron microscope (SEM) image of an example fabricated XCSEL. There is a conventional lateral current injection layer of around 3 µm thickness visible in the image which is actually not needed. Typical values for the lateral etch depth under the edge of the resist mask are 20 µm and 30 µm. The former produces a smaller sidewall notch and leaves a portion of the top mirror with more or less vertical sidewall as in Fig. 2, while the latter value produces notches spanning the entire top mirror. A mask was designed for arrays with 4×8 elements and 8 different VCSEL sizes with diameter increments of 2 µm.

3. Self-Aligned Hybridized XCSEL Arrays

An overview of a complete substrate-side-emitting flip-chip XCSEL structure is displayed in Fig. 3. Remarkably, despite of its complex shape, this structure takes much less effort to make than previous versions of flip-chip VCSELs. In the final state shown in Fig. 3, all of the substrate is removed, reducing the XCSEL to only the cavity and mirror layers. Prior to the injection of an underfill, the structure is free-standing, however stable enough for normal laboratory handling while measurements are performed. In order to demonstrate how far the XCSEL approach can be taken, the devices were fabricated with integrated mechanical guides to aid the alignment of optics. There is also an efficient through-connection for the bottom contact.

A main characteristic of XCSELs is the strongly improved thermal management. While all direct-mesa solder-bonded VCSELs have a good thermal connection of the mesa top to the solder joint, in XCSELs the top distributed Bragg reflector (DBR) sidewalls are also wrapped with metal without any passivating, and hence heat-blocking, interlayers. However, the biggest gains in heat flux in XCSELs versus conventional VCSELs are expected by the heat spreaders leading from the central cavity over the sidewalls of the bottom DBR to the optically contacted side of the lasers. These heat spreaders immediately access the inner heat source and transport heat away from there toward the optical side of the chip stack. This is the side that lends itself to cooling, since passive optics do not emit any additional heat.

In XCSELs, initially created profiles in the wafer surface are the basis for all subsequent processes. These profiles are the result of two lithography and subsequent wet-etching steps. Along with the actual laser profiles, spikes are created that lack any overhangs in their sidewalls. Once the profile is created and metal covered for electrical and thermal

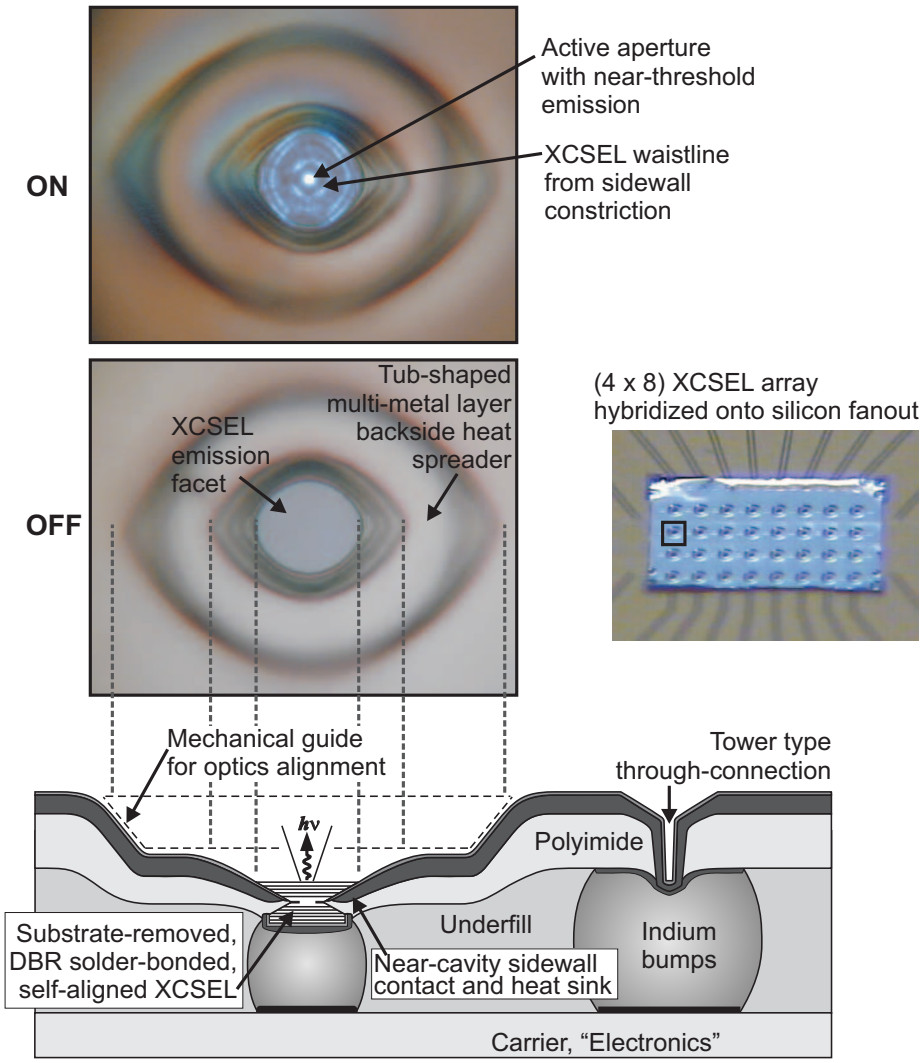

Fig. 3: Overview of the fabricated structure: fully self-aligned direct-mesa solder reflow flip-chip bonded 4×8 XCSEL array, each laser including an optics alignment guide. The schematic at the bottom gives a cross-section of one cell in the hybridized laser array that is shown after placement onto a silicon carrier with address lines in the right-hand photograph. The left-hand photographs are close-up views of the emission side of one XCSEL in this array, both in off and on state.

conduction, the procedure that provides the flip-chip interfaces is simple: the entire surface structure is cast in a single layer of a suitable polymer. After the polymer is hard-baked, it is plasma-etched to simultaneously expose the XCSEL top DBR and the top of the through-connection towers.

Conventional processing methods are employed to implement the flip-chip interface. The left-hand image of Fig. 4 shows the plated solder pads wrapped around the XCSELs and through-connections while still embedded in the plating resist. The two images to the right show the pads after resist removal. The plating base is still present in these images. Eventually the solder is deposited in the same way as was explained in [5] to provide flip-chip-ready lasers.

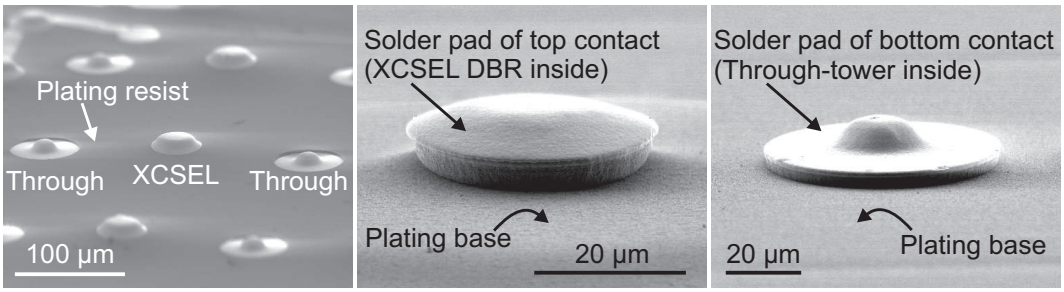

Fig. 4: SEM images of about 5 µm thick plated solder pads wrapped around the top parts of the XCSELs and through-connections. In the left-hand image the pads are still embedded in the plating resist while in the two images to the right the resist has been removed.

4. Experimental Results

4.1 Thermal properties

Appropriate heat management is a key to VCSEL performance, for which the thermal resistance is a convenient global measure. It is defined as $R_{\mathrm{Th}} = \Delta T / P_{\mathrm{diss}}$, where ΔT is the average temperature increase and P_{diss} is the dissipated power in the device. Except for thermal tuning schemes, a low thermal resistance is normally desired to limit self-heating. This permits efficient high-current operation throughout the operating life. In high-speed applications, excessive junction temperatures cause the resonance frequency to saturate. In many instances such as the direct flip-chip integration of VCSELs to electronic circuitry, the lasers are attached to hot surfaces and cannot rely on active cooling through a heat sink. That is, they are densely integrated with other heat sources rather than with heat sinks. When many heat sources are densely packed, the overall package has to ensure efficient heat flow.

Figure 5 provides an overview of thermal resistances for a large range of devices. Extensive data from previous works is included for comparison (sorted by year): Lear1995 [6], Mathine1996 [7], Wipiejewski1996 [8], MacDougal1998 [9], Pu1999 [10], Krishnamoorthy2000 [11], Teitelbaum2004 [12], Al-Omari2005 [13], Al-Omari2006 [14], Demir2011 [15]. U-L-M2007 is a typical value for commercial oxide-confined on-substrate devices. Very low thermal resistance values were reported more than a decade ago [8] for on-wafer-measured air-post devices, where the active diameter is defined by the diameter of the pillar etched into the top DBR. These devices retained their substrate through which the backside contact is provided. They are apparently not fully isolated, since the bottom DBR as well as the active region layers were left untouched. This structure was buried under 15 µm of plated Au spanning an area of $300 \times 300\,\mu\mathrm{m}^2$ for heat spreading, and thereby creating a large interface with the opposite polarity DBR, which precludes high-speed modulation for data transmission.

High-speed devices with conventional sidewall heat spreaders were more recently fabricated with the objective of lowering the thermal resistance by sidewall heat extraction. The oxide-confined devices in [13] are 850 nm top-emitting on p-substrate and have a copper heat sink on 200 nm of SiN_x wrapped around dry-etched mesas. In [14], a similar

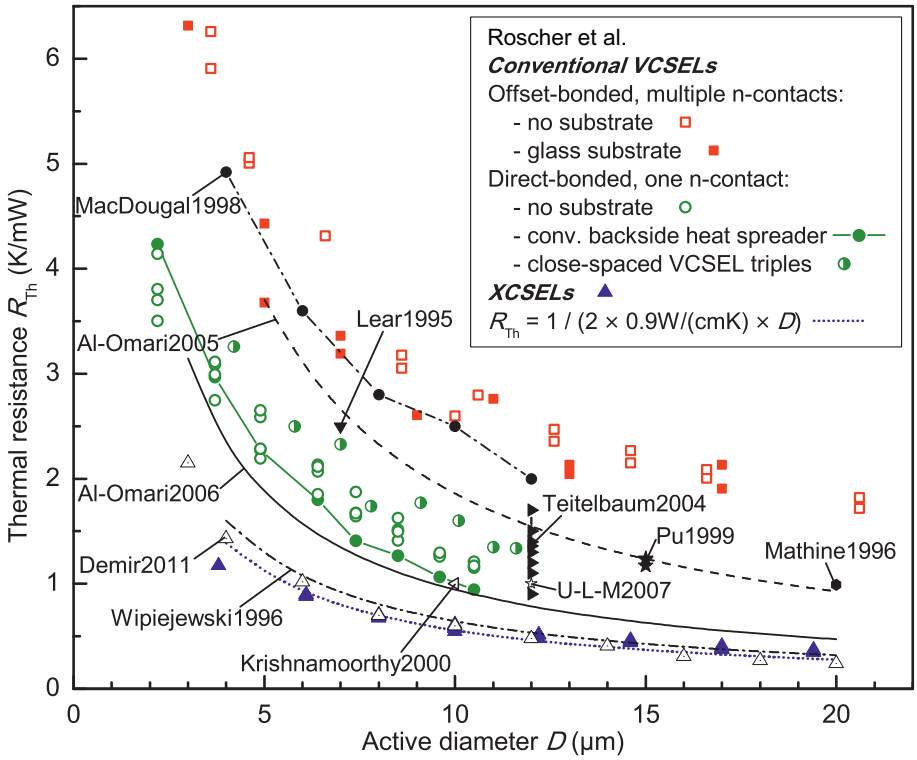

Fig. 5: Overview of thermal resistances achieved for many device configurations. For comparison, data from previous works is included, indicating the first author and year of publication for convenient reference. Corresponding publications are provided in the text.

configuration is used for 980 nm top-emitting VCSELs on n-type substrate. The lasers directly measured on-wafer showed bandwidths up to 16 and 10 GHz, respectively.

Not many details about the "lithographic VCSEL" structure (Demir2011 data in Fig. 5) are revealed in [15], except that these devices are oxide-free. The thermal resistance values were measured on-wafer with thermal power dissipation through the native substrate. These devices are not implemented in a hybridized array configuration. Their modulation properties are not demonstrated.

Even with the early fabricated XCSELs, the thermal resistances were cut by half with respect to previous direct-mesa-bonded VCSELs (see the circles in Fig. 5). These are the best values achieved to date and they even compare favorably with the values of devices from [8] that are aggressively designed for low thermal resistance, have a much less complex structure, and are not capable of any high-frequency modulation. Since then, VCSEL technology has seen the introduction of oxide apertures, hybridization techniques including flip-chip bonding and substrate removal, all of which are used for high-speed applications. XCSELs incorporate this, cut down on processing effort, and bring the thermal resistance to extremely low values, for instance to 0.55 K/mW for a 10 µm active diameter device. The full upright triangles in Fig. 5 show 26 XCSELs indicating good consistency.

In order to obtain the simple analytical expression [16] $R_{\mathrm{Th}} \approx 1/(2\lambda_{\mathrm{c}}D)$ for the thermal resistance in Fig. 5, the VCSEL structure is assumed to be a small disk with diameter D

from which heat flows into a half-space filled with material of thermal conductivity λ_c, where D is taken to be the active device diameter and λ_c is mainly determined by the substrate or heat sink materials. According to the dotted curve described by this equation (see the inset of Fig. 5), this frequently applied law still describes the behavior quite well, given the fact that the actual configuration has little resemblance with the underlying model. It seems, however, to overestimate the increase in R_{Th} as the devices shrink in size and active diameters. Apparently, heat extraction through the circumference of the active region by sidewall heat spreaders becomes more important as the diameters shrink. This is even more true for these devices, since they had a large spread of oxidation lengths, with 4.5 µm for the largest and 5.5 µm for the smallest XCSELs, an about 30 % increase due to the stronger curvature of the oxidation front. A better fit of the data would be achieved if an exponent were included in the denominator of the equation. However, this is avoided since with its present form, an effective material conductivity, with which the imaginary half-space should be filled to achieve the same heat flow from a point heat source, can be derived. With 0.9 W/(cm K), this effective conductivity is about twice as large as that of GaAs (0.45 W/(cm K)), which demonstrates the effectiveness of heat transport in XCSELs.

4.2 Static and dynamic performance

An exemplary XCSEL with 7 µm active diameter has a threshold current of 1.6 mA. After normal processing, ending with substrate and etch-stop removal, the device has a differential resistance of approximately 110 Ω in the current range between 5 and 15 mA. The differential quantum efficiency is 65 % and roll-over occurs at 17.1 mA with 10.1 mW maximum output power. The emission spectrum is similar to that of conventional multimode VCSELs. The far-field profile shows a typical donut-like shape that is a consequence of current crowding and spatial hole burning, leading to preferential pumping of higher-order modes.

Beside having produced the best thermal performance so far demonstrated for this device configuration, XCSELs show attractive dynamic properties. For testing the dynamic performance of flip-chip bonded XCSELs, a carrier is required with transmission lines to address each device. The effects of these lines are contained in the results, since no means were readily available to characterize them separately for de-embedding purposes. An early design of a 4×8 carrier was employed for all XCSEL measurements, whose transmission lines were intended for much lower frequencies than are achievable with today's devices. Moreover, this carrier has large bond pads with 60 µm diameter. For the reflow flip-chip soldering to work properly, evenly large bond pads had to be placed over the XCSELs and an appropriate amount of indium solder deposited. These large pads introduce capacitance, while they are not responsible for the good thermal performance since the solder joint cross-section has not been identified as major bottleneck for heat transport.

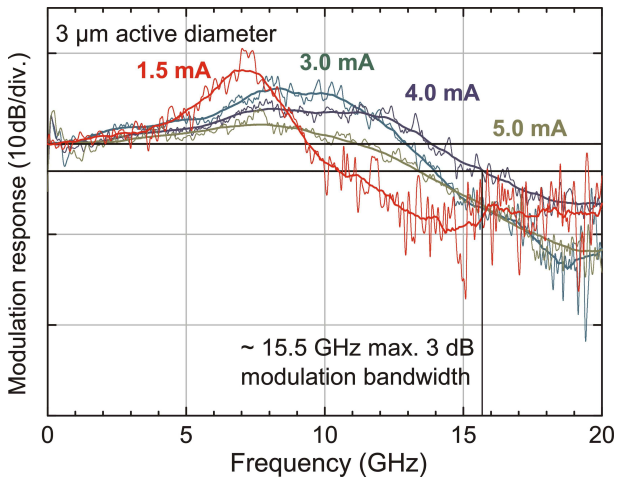

Fig. 6: Small-signal modulation transfer functions of an XCSEL on an early silicon carrier for different operating currents above threshold.

Figure 6 shows the measured small-signal modulation transfer functions for different currents I. Adjacent averaging has been applied to the as-measured curves (thinner lines) to obtain the smoothed curves (thicker lines) that help to determine the corner frequencies. The XCSEL has an active diameter of 3 µm, a large oxidation length of 13 µm, and large 60 µm diameter bond pads. A maximum 3-dB modulation bandwidth of around 15.5 GHz is achieved at 4 mA drive current. From the curves one can extract the corner frequencies $\nu_{3\,\mathrm{dB}}$ as a function of $\sqrt{I - I_{\mathrm{th}}}$, and with a threshold current $I_{\mathrm{th}} = 1\,\mathrm{mA}$ obtain a modulation current efficiency factor $\mathrm{MCEF} = \nu_{3\,\mathrm{dB}}/\sqrt{I - I_{\mathrm{th}}}$ of approximately $8\,\mathrm{GHz}/\sqrt{\mathrm{mA}}$.

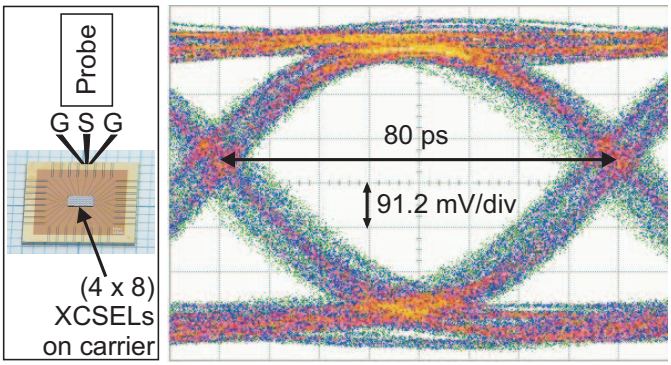

Fig. 7: Photograph of the XCSEL array on a carrier fanout chip with a schematic contact arrangement of a microwave probe (left) and 12.5 Gbit/s eye diagram for modulation with a $2^7 - 1$ word length pseudorandom bit sequence (right).

For testing under digital modulation, only a 12.5 Gbit/s bit pattern generator was available. Figure 7 depicts an optical eye diagram recorded at this data rate. The XCSEL was operated at 3.5 mA bias current and modulated with a peak-to-peak voltage of 1.5 V. While the slow rise and fall times are attributed to the limited receiver bandwidth (an 8 GHz photoreceiver and a 10 GHz amplifier were employed), the eye diagram demonstrates that these devices are suitable for digital data transmission applications at these bit rates. The left part of Fig. 7 shows the entire XCSEL array and the flip-chip carrier described above.

5. Conclusion

We have introduced a novel fabrication approach to flip-chip-bondable 850 nm VCSELs and one- or two-dimensional VCSEL arrays. A unique sequence of wet-etching steps allows us to deposit contact metals close to the region of major heat generation, which reduces the thermal resistance to much improved levels compared to conventional substrate-less VCSELs. Simultaneously the etching sequence readily establishes a flip-chip interface and a surface topology which might prove useful for direct butt coupling to arrays of optical fibers. Fully functional arrays of such XCSELs have been fabricated and equipment-limited digital modulation at 12.5 Gbit/s was demonstrated.

It is worth to point out that the epitaxial layer sequence used for XCSEL production has not been optimized for high-frequency operation. We believe the increase in modulation bandwidth we have seen in XCSELs compared to conventional VCSELs (that were fabricated with similar epitaxial material) is a result of better thermal management that does not interfere with high-frequency circuit properties. The present data were obtained with largely non-ideal devices. Immediate improvements are evident with minimized oxide widths, adjusted bond pad sizes, and shorter address lines on the carrier. Moreover, with common techniques like quantum well strain engineering or photon lifetime adjustment, we can expect that there is much room for improvements of the laser dynamics.

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