



Trigger Systems Reconfigurable Computing in Experimental Physics

Andrea Triossi

October 2009, CHR working week, University of Ulm







Trigger systems overview

Trigger systems examples

•	Compact	Muon	Solenoid	(CMS)
---	---------	------	----------	-------

Advanced Gamma Tracking Array (AGATA)

Formal description

- Property Specification Language (PSL)
- Automatic Synthesis

act Muon Solenoid (CMIS)	@ CERN

@ GSI

Trigger in Physics Experiments

INFN Istituto Nazionale di Fisica Nucleare





Trigger implementation

General requirements

- Low latency: few µs
- Output rate 100 KHz ÷ 1MHz
- Large degree of parallelism
- Dead time free operation





- Flexibility
- Pattern matching algorithms
- High number of channels



CMS: Muon Drift Tube









Size: 21 m long 15 m wide 15 m high Weight: 12 500 tones Location: 100 m underground inside LHC tunnel





Track selection based on the best track quality and higher transverse momentum

AGATA Experiment







 4π array of HPGe detectors for in-beam γ -ray spectroscopy 36 fold segmented crystal + central core contact (6660 channels)

Digital electronics and sophisticated Pulse Shape Analysis algorithms Operation of Ge detectors in position sensitive mode $\rightarrow \gamma$ -ray tracking

AGATA: Global Trigger System







User defined trigger rules range from simple multiplicity conditions in independent partitions to more complex delayed coincidences involving two or more partitions



Formal description of trigger





- To search for multiplicity conditions in independent partitions during a fixed time window or delayed coincidences involving more partitions
- Integration on multiple channels with threshold comparison
- > To look in a small database of predefined patterns for a complete or partial matching with the recorded values





Necessity \rightarrow formula will be always true in the futurePossibility \rightarrow formula will be eventually true in the future Modal Logic \prec



Property Specification Languagen FN





SystemVerilog – Verilog VHDL – SystemC – GDL



Assertion-Based Verification







Testbench > Design Lack of suitable debugging tools





Constraint Handling Rules



Hardware elements

