On Incremental $\Delta \Sigma$ Modulators with SNR and SQNR Enhancement by Recuperation Phase

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Abstract—This paper presents a system-level technique that is capable of enhancing the efficiency of high-resolution incremental delta sigma (I-$\Delta \Sigma$) modulators. With little additional effort in circuitry it is possible to make use of a recuperation phase in which the I-$\Delta \Sigma$ modulator’s input is periodically tied to a defined reference. In these phases, the modulator is given time to adjust its residual error to a minimum. This method is capable of increasing the maximum stable amplitude (MSA) as well as the signal-to-quantization-noise ratio (SQNR). Consequently, all measures to restore the efficiency of incremental $\Delta \Sigma$ parameters. Though, the efficiency of an I-$\Delta \Sigma$ modulator operates with an order modulators as an increase in these measures directly affects power requirements. The method is analytically derived and exemplarily simulated. Furthermore, a circuit-level simulation in a 180 nm CMOS technology node is presented to validate the presented results.

I. INTRODUCTION

$\Delta \Sigma$ ADCs are preferred candidates for high-resolution analog-to-digital converters for low to medium speed signals due to their inherent properties like oversampling and noise shaping which trade speed for accuracy. Nevertheless, these ADCs can not be used in multiplexed environments due to their memory which is inherent to the system. Incremental $\Delta \Sigma$ (I-$\Delta \Sigma$) ADCs are able to close this gap. These ADCs are operated like their freely running counterparts, but are reset after a number of M cycles. Thus they offer a true Nyquist-rate behavior which is a factor of the oversampling ratio (OSR) times lower than the internal sampling speed. Additionally, this type of ADC requires a different digital filter than freely running $\Delta \Sigma$ converters. Theoretically, a brickwall filter can be used for evaluating freely running ones whereas a resettable reconstruction filter should be used to calculate the digital estimate of the input signal from the digital output sequence of an I-$\Delta \Sigma$ modulator [1]. The periodic reset of the I-$\Delta \Sigma$ ADC makes it possible to use a single ADC for converting multiple channels leading to significant power and area savings at the same time by properly choosing system parameters. Though, the efficiency of an I-$\Delta \Sigma$ ADC compared to its freely running counterpart decreases due to its operation in transient mode meaning more OSR is needed for similar SQNR. Consequently, all measures to restore the efficiency of this type of ADC are highly demanded.

In this paper, a technique is presented which makes use of the control-loop-like behavior of the I-$\Delta \Sigma$ ADC by switching off the input to a reference such that the residual error within the system can be reduced to a minimum. Therefore, Section II introduces the measures that are necessary to evaluate the effect of signal gating and the recuperation phase (RP) method. Section III evaluates the effect of the proposed RP method for an exemplary 3rd order I-$\Delta \Sigma$ ADC designed for the multiplexed digitization of biosignals. In Section IV the circuit-level simulations are discussed. Subsequently, Section V presents the achieved improvement in performance making use of the RP method. Section VI concludes the results.

II. BASIC OPERATION OF I-$\Delta \Sigma$ ADCS

The block diagram shown in Fig. 1 depicts the operation principle of a discrete-time (DT) I-$\Delta \Sigma$ modulator. The continuously running input signal $u(t)$ is sampled by the switched-capacitor (SC) network of the first integrator stage of the modulator. An input sample and hold (S&H) is assumed in the subsequent derivation. It can be omitted as the signal is only slowly varying as compared to the internal sampling speed $f_s$. Nevertheless, this leads to a modified analog input-to-digital output transfer function which shows lowpass characteristic as described in [2]. The I-$\Delta \Sigma$ modulator operates with an internal sampling rate of $f_s$ which is M times higher than the digital Nyquist-rate output $D_n$. In every cycle the modulator produces a digital output $d[k]$. The modulator can be regarded as an encoder that changes the analog input signal into a digital code sequence $d[k]$. Therefore, a digital reconstruction filter with transfer function $h[k]$ is needed to synchronously decode this sequence such that an accurate digital representation $D_n$ of the input is found. Such a digital filter can be as simple as a cascade of integrators (CoI) filter of the same order as the modulator to match the integrator chain of the modulator.
Other implementations like the optimal filter [3] are possible at the cost of an increased complexity of the digital system. The modulator as well as the reconstruction filter are entirely reset after a number of M cycles. The \( n^{th} \) Nyquist-rate sample is taken right before the reset.

In the following, the basic analysis of an I-\( \Delta \Sigma \) modulator is presented which is needed to follow the derivation of the proposed RP method. For the sake of simplicity, the equations are derived for a 1\(^{st}\) order modulator, as depicted in Fig. 2. In the following it is assumed that the modulator features a low-distortion path from input to quantizer resulting in a unity STF for inband signals. Thus, the overall transfer function is solely defined by the digital reconstruction filter \( b[n] \).

The output of the integrator \( r[k] \) at the end of the discrete-time instant \( k = m \) in the \( n^{th} \) Nyquist-rate conversion cycle can be calculated as

\[
\begin{align*}
\text{r}_n[m] &= m \cdot u[n \cdot M + 1] - \sum_{k=n \cdot M+1}^{n \cdot M+m} d[k]. \quad (2)
\end{align*}
\]

It is assumed that the reset takes place during an infinitely small time instant at the end of the last conversion cycle. Furthermore, it is assumed that the input \( u[k] \) is constant for a whole Nyquist-rate conversion cycle. Under this condition

\[
\text{r}_n[m] = m \cdot u[n \cdot M + 1] - \sum_{k=n \cdot M+1}^{n \cdot M+m} d[k]. \quad (2)
\]

Assuming stable operation, the output of the integrator is bound at any time instant \( m \) during any Nyquist-rate conversion cycle, which leads to the following inequality [4]:

\[
\frac{V_{\text{ref}}}{m} \geq \left| u[n \cdot M + 1] - \sum_{k=n \cdot M+1}^{n \cdot M+m} d[k] \right|. \quad (3)
\]

Here \( V_{\text{ref}} \) is the reference voltage. Looking at Fig. 2, the decimated and scaled digital output of the \( n^{th} \) Nyquist-rate conversion cycle at time instant \( k = m \) can be calculated as

\[
\text{D}_n[m] = \frac{1}{m} \sum_{k=n \cdot M+1}^{n \cdot M+m} d[k]. \quad (4)
\]

Ideally the decimated digital output sample of the \( n^{th} \) Nyquist-rate conversion \( D_n \) would match the input sample at the beginning of a Nyquist-rate conversion cycle. This can not be the case for a finite OSR at the presence of quantization errors, circuit non-idealities and noise. Nevertheless, it is desirable that the error

\[
u[n \cdot M + 1] - D_n \rightarrow 0. \quad (5)
\]

Using equation (4) in (2) matches (5) for \( m = M \) and \( r_n[M] \rightarrow 0 \). This leads to the conclusion that the error of an I-\( \Delta \Sigma \) modulator is visible at the output of the last integrator. Without the loss of generality, this consideration is valid for higher order systems if the residual error is scaled accordingly by the respective integrator coefficients. This property is exploited in systems that make use of extended counting [5]. Referring the error voltage at the output of the last integrator to the digital output by dividing by the respective filter weight and the integrator coefficients gives the remaining output-referred quantization error of the ADC.

### III. PROPOSED RECUPERATION PHASE METHOD

As in any control system, the impulse response is defined as the reaction of the system’s output to external excitation. In the case of the I-\( \Delta \Sigma \) modulator, the quantization error as a reaction of an impulse at the input is of interest. Thus, any excitation of the input will lead to a response of the loop such that the quantization error \( r[k] \) can never reach a steady state, which should ideally become zero. The idea of the recuperation phase is to use the last part of every conversion for modulator recuperation, during which the modulator can further reduce the remaining quantization error without input disturbance. Therefore, the input of the modulator is disconnected from the signal and tied to a defined voltage for a certain number of cycles. It can be shown that the best results are achieved by tying the input voltage to any of the thresholds of the quantizer. The optimal length of this phase depends on the selected modulator architecture, the order, as well as the aggressiveness of the scaling of the coefficients, which affect the loopfilter transfer function. In order to determine the optimal length of the recuperation phase, a particular architecture has to be chosen, simulated and analyzed.

As an example, we have chosen an I-\( \Delta \Sigma \) ADC which is suitable for the processing of biosignals with large dynamic range. An SNR \( \geq 94 \text{dB} \) is targeted. Moreover, the ADC should be able to be multiplexed between exemplarily 10 electrodes, each having a signal bandwidth of 10 kHz which leads to a Nyquist-rate \( f_s=200 \text{kS/s} \). A 3\(^{rd}\) order CIFF \( \Delta \Sigma \) architecture including a low-distortion path is chosen using a single-bit quantizer for inherent DAC linearity. The resulting exemplary modulator is shown in Fig. 3. The order of the CoI reconstruction filter matches the order of the modulator. The coefficients are derived with the help of a genetic algorithm as used on www.sigma-delta.de [6]. The used scaling coefficients are shown in Table I. Extensive simulations show that an OSR of 160 is necessary to obtain an SQNR of \( \geq 100 \text{dB} \), which is necessary to achieve a circuit noise dominated SNR\( \geq 94 \text{dB} \).

<table>
<thead>
<tr>
<th>( a_1 )</th>
<th>( b_1 )</th>
<th>( b_4 )</th>
<th>( c_1 )</th>
<th>( c_2 )</th>
<th>( d_{13} )</th>
<th>( d_{23} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2393</td>
<td>0.2393</td>
<td>1.0000</td>
<td>0.4309</td>
<td>0.9169</td>
<td>9.7523</td>
<td>8.9423</td>
</tr>
</tbody>
</table>

Simulations for 3 distinct values of the RP are performed...
to see how the output referred quantization error behaves during a single Nyquist-rate conversion cycle. This error is calculated by sweeping the input signal amplitude from 0 to the MSA and calculating the rms value of the output of the last integrator individually for every time instant $k$ during a Nyquist-rate conversion cycle. To refer this error to the output it is furthermore divided by a factor $F[k]$ for every individual time instant $k$. This factor $F[k]$ is only valid for $k > 3$ due to the delay within the filter. It can be calculated for the exemplary modulator as:

$$F[k] = \frac{1}{b_1 \cdot c_1 \cdot c_2 \cdot (k-1) \cdot (k-2) \cdot (k-3)}.$$  \hspace{1cm} (6)

The results are shown in Fig. 4. It can be seen that for the common operation without RP, the quantization error steadily decreases over operation time until the final cycle. Interestingly, the quantization error rapidly drops at the beginning of a RP and then steadily decreases again towards the end of a conversion. For the three shown distinct RPs in Fig. 4, it should be noted that the new trendline for the quantization error is the same irrespective of the start of the RP. The steady decrease after the sudden drop in the quantization noise shortly after the start of the RP goes along with the modulator running again into limit cycles, after which no dramatic decrease in quantization noise is visible. To select the optimal time instant for tying the input to a defined value and give the modulator time to recuperate, another side effect of this method has to be taken into account. Simultaneously, by tying the input to zero, no signal is fed to the modulator and digital filter anymore. This means that the effective output signal amplitude is attenuated by

$$\alpha = 1 - \frac{(R-1) \cdot (R-2) \cdot (R-3)}{(M-1) \cdot (M-2) \cdot (M-3)}$$  \hspace{1cm} (7)

where $R$ denotes the length of the RP and is assumed to be larger than 3 to pass the digital filter. Fig. 5 shows the attenuation of the output signal amplitude due to the signal gain $\alpha$ introduced by the reconstruction filter for different RP lengths, where the RP starts $R$ clock cycles prior to the end of every single Nyquist-rate conversion. Obviously, the RP length should be kept small to limit its influence as circuit noise is not attenuated during the RP.

The maximum stable amplitude of any $\Delta \Sigma$ modulator gives an upper limit for the maximum amplitude of the input signal that can be applied to the modulator before overload starts to significantly impact the achievable resolution. Generally, a large MSA is important since for a required SNR, the MSA defines the allowable input referred noise, and the latter sets the requirements on sampling capacitor size, input stage thermal and 1/f noise, etc. Consequently, increasing the MSA directly yields smaller size and power consumption of the I-$\Delta \Sigma$ modulator. By switching off the input signal, the modulator is given time to stabilize as no additional signal power is injected into the system anymore. Therefore, it seems reasonably conclusive that a larger amplitude for the cycles before the RP can be tolerated without driving the modulator into overload towards the end of the Nyquist-rate conversion cycle. Fig. 6 shows the simulated MSA for different lengths of RPs. It can be seen that, by allowing a RP, the MSA of the exemplary 3$^{rd}$ order, single-bit I-$\Delta \Sigma$ modulator can be extended by around 2 dB while, as shown in Fig 4, also the quantization noise is reduced. Thus, both the SQNR and the MSA are improved by the proposed RP.

### IV. Circuit Design

The circuit design for this exemplary modulator was carried out in a 180 nm CMOS technology with a supply voltage of $V_{DD} = 3 \, \text{V}$ and a common-mode voltage of $V_{CM} = 1.5 \, \text{V}$, respectively. The 1$^{st}$ integrator stage of the fully differential modulator is the most demanding because it must meet the
noise and linearity requirements of the entire system. Non-idealities in the 2nd and 3rd stage are suppressed by the first stage and thus the requirements on these stages are significantly relaxed. Consequently, the first stage is implemented as a folded cascode amplifier with slew rate enhancement whereas the 2nd and 3rd integrator are implemented as plain telescopic amplifiers with much smaller sampling and feedback capacitor sizes, respectively. The switches in the SC network at the input of the first OTA are the most critical as their linearity directly affects the overall linearity of the system. Bootstrapped switches are used in the first and second SC stage, respectively. The signals are added inside a latched comparator by having weighted input transistors operating in the linear region as presented in [2]. The SNR of the circuit-level modulator is mainly determined by the input sampling capacitor \( C_s \), which due to the oversampling nature can be approximated by

\[
P_{\text{noise}} \propto \frac{k_b T}{C_s \cdot M} \tag{8}
\]

according to [7] where \( k_b \) is the Boltzmann constant and \( T \) is the temperature. For the exemplary design, \( C_s \) has been chosen 300 fF to meet the target of SNR \( \geq 94 \) dB, while all other noise sources have been excluded from simulation. By using the proposed RP for a length of 25 cycles and increasing the maximum stable amplitude by 2 dB, the sampling capacitor size could theoretically be reduced by 36% if only the thermal noise contribution of the input SC network is considered. Consequently, also the integration capacitor of the first stage can be reduced by the same amount, which allows to reduce current and \( g_m \) needed for SR and GBW of the first integrator.

V. SIMULATION RESULTS

Simulating the circuit-level modulator for a sinusoidal input signal with an input amplitude of \( V_{\text{in, dif}} = 1.8 \) V at a frequency of 10 kHz using the previously described parameters and coefficients but without the RP method, leads to an SNR of 94.7 dB. Making use of the proposed RP method and switching the input to VCM for the last 25 cycles of each Nyquist-rate conversion allows to increase the input amplitude to \( V_{\text{in, dif}} = 2.4 \) V leading to an SNR of around 97.9 dB. This makes it possible to reduce the sampling capacitor \( C_s \) by 48% as confirmed by a simulation shown in Fig. 7. This even exceeds the approximated 36% as the RP method does not only allow for a larger MSA but also reduces quantization noise at the same time which allows even slightly more contribution from the sampling capacitor. This decrease in \( C_s \) directly leads to power savings in the first, power hungry integrator and is therefore a great measure of improving the efficiency of the modulator, which validates the usefulness of this easy to use technique of RPs in I-\( \Delta \Sigma \) modulators.

VI. CONCLUSION

In this paper, a new system-level technique especially suited for high-resolution, low power I-\( \Delta \Sigma \) is presented. The novelty in this design is the RP method that allows to reduce the internal quantization error and increase the MSA at the same time, thereby increasing the efficiency and resolution of a system without excessive circuit effort and without the need for more power in the OTAs. Another benefit for the usage of an I-\( \Delta \Sigma \) employing this technique is the fact that preceding circuitry driving the modulator can be deactivated during the RP thereby further reducing the power consumption of a system that integrates such an ADC. Regarding the simulation results including the RP method, the proposed ADC is able to reduce the input sampling capacitor by 48% which directly leads to tremendous power savings in the first integrator and therefore of the whole ADC.

REFERENCES