High Power $3 \times 3$ VCSEL Array

Michael Miller, Martin Grabherr

We have fabricated high power and highly efficient bottom-emitting $3 \times 3$ VCSEL arrays with an optical output power of 650 mW under cw operation at room temperature. The maximum spatially averaged power density is 370 W/cm$^2$ for the total chip size of $420 \times 420 \mu m^2$ for the cleaved array. This requires an improved mounting technique for efficient heat sinking of the devices.

1. Introduction:

Vertical cavity surface emitting lasers (VCSELs) have become superior devices for various applications in data transmission, especially parallel optical interconnects. Their output power is limited to a few mW due to the small active diameter of about 10 $\mu m$ and thermal rollover. To obtain higher optical power one can increase active size of a single laser at the cost of decreasing wallplug efficiencies [1] or switch to two-dimensional arrays which provide high output powers at still high conversion efficiencies [2]. For both conceptions improved heat sinking of the devices is indispensable.

2. Devices:

Fig. 1. Schematic drawing of a two-dimensional bottom emitting VCSEL array soldered on diamond heat spreader.

We have designed and fabricated efficient VCSEL arrays consisting of $3 \times 3$ bottom-emitting devices for a wavelength of 980 nm. The structure shown in Fig. 1 is grown by solid source MBE and consists of 30 p- and 24 n-type Bragg-reflectors surrounding the inner cavity with three 8 nm thick InGaAs quantum wells. 70 $\mu m$ diameter mesas are wet chemically etched down to the depth of the inner cavity and
current apertures of 50 μm in diameter are formed by wet oxidation of a 30 nm thick AlAs-layer just above the p-type cladding layer. The center to center spacing between neighboring elements is 140 μm. Evaporation of the p-type contact is followed by deposition of a passivation layer on the epitaxial side. After thinning of the substrate to a thickness of around 180 μm an anti-reflection coating is sputtered. To structurize the emission-windows a dry etching step with CAIBE is done. The n-type contact is then evaporated and structured by lift-off technique and a 1 μm thick Au-layer is deposited galvanically for bonding. Finally, the cleaved arrays are soldered junction side down on diamond heat spreaders and heatsunk on copper submounts. The characteristics of good soldering are mechanical stability and good thermal and electrical contacts. Therefore an eutectic AuSn-alloy consisting of 80% Au and 20% Sn is used as a hard solder. The array is mounted using a Die Bonder. The thickness of the solder is 5 μm which is quite large. Various tests have shown that it can be reduced below 2 μm. There are many influences during the soldering process like pressure, atmosphere, temperature and time. Fig. 2 shows the surface of a metallized diamond with solder on it after an array was soldered and removed again. The maximum temperature and the soldering time were not well adjusted so in the impressions from the mesas a lot of airholes can be seen which causes insufficient thermal contact and bad mechanical stability. In spite of these bad conditions an increase in the optical output power can be seen but there is still place for improvements. After several tests it was possible to achieve a good soldering which can be seen in Fig. 3. Again an array was soldered and removed afterwards but now the soldering interface is intact. The mesas were torn off where the current aperture was oxidized and one can see the broken crystal structure.

3. Measurements:

The output characteristics of the individual elements from the 3 × 3 array are given in Fig. 4. The threshold current is about 17 mA which gives a threshold current density of about 870 A/cm². The maximum output power range is between 55 and 65 mW and the maximum conversion efficiency is between 32 and 36% at 3 times threshold. The differential resistance is 8.9 Ω. Due to the common p-contact after mounting the array on the diamond heat spreader all the elements have to be driven parallel. Therefore a good homogeneity of the elements in the array is necessary which can also be
seen in Fig. 4. This results in an overall output power of 650 mW at about 9 times threshold and 15% conversion efficiency under cw operation. The LIV curves in Fig. 5 show a threshold current of 153 mA corresponding to 9 times the threshold of an unmounted individual device. Threshold voltage and differential resistance are 1.8 V and 1.4 Ω, respectively. The slight increase of the differential resistance for the parallel driven devices is due to the not perfect soldering on the diamond. Maximum conversion efficiency reaches 25% at 3.2 times threshold at an output power of 270 mW. The maximum spatially averaged power density is 370 W/cm² for the total chip size of 420×420 μm² for the cleaved array.

4. Outlook:

Further investigations will be done for larger arrays with more elements and a higher density. Therefore the soldering technique has to be investigated in detail. Very important for densely packed VCSEL arrays is the thermal cross talk between the elements. To get more information about this, independently addressable elements in an array are requested. This can be done by using structured heat sinks.

References
