

2D VCSEL Arrays for Chip-Level Optical Interconnects

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Oxide-confined vertical cavity surface-emitting laser diodes (VCSELs) are fabricated for applications in chip-level optical interconnects. 980 nm wavelength devices in arrays with 4×8 elements are investigated. Threshold voltages of 1.5 V and operation voltages below 2 V of submilliamp threshold current lasers are fully compatible to 3.3 V CMOS technology. Modulation bandwidths of 9.5 GHz at 1.8 mA laser current with a modulation current efficiency factor (MCEF) of $10 \text{ GHz}/\sqrt{\text{mA}}$ is demonstrated for $3 \mu\text{m}$ diameter VCSELs. No error floors are observed down to bit error rates (BERs) of 10^{-11} at 12.5 Gb/s data transmission.

1. Introduction

Parallel optical links will penetrate more and more into areas such as inter-cabinet and inter-board down to intra-board data communication, nowadays mostly dominated by electrical interconnect solutions. In recent years, one-dimensional parallel datacom links have accelerated progress in optical interconnect technology [1] but the hardware is too bulky and the aggregate bit-rate is far too low for chip-level interconnects. In order to satisfy the increased need for data throughput per area in chip-level links two-dimensional (2D) interconnects and integrated wiring-technologies such as flip-chip bonding are necessary. The left-hand side of Fig. 1 shows a schematic of a parallel optoelectronic interconnect on chip-level. Source and detector chips are directly bonded onto Si CMOS chips and the optical datastream is transferred from one chip to another chip using free-space optics or 2D waveguide arrays.

The right-hand side of Fig. 1 shows a photograph of a fabricated transmitter chip where a bottom-emitting VCSEL array with 4×8 elements is flip-chip mounted on a $0.8 \mu\text{m}$ CMOS driver chip [2]. Due to their high efficiency at low driving currents, high-speed data transmission capabilities and the possibility of 2D array fabrication as well as the intrinsic compatibility with fiber and free space optics VCSELs are regarded as a key enabling technology for low-cost chip-level optical interconnects.

2. Chip Fabrication and VCSEL Characteristics

The left-hand side of Fig. 2 shows a photograph of a $150 \mu\text{m}$ thick bottom emitting VCSEL array. The active region of an individual laser is formed by three 8 nm thick compressively strained $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum wells embedded in GaAs barriers for 980 nm emission wavelength. The inner cavity is sandwiched between an upper p-doped and a lower n-doped Bragg reflector, consisting of 20.5 and 30 quarter-wavelength GaAs/ $\text{Al}_{0.88}\text{Ga}_{0.12}\text{As}$ layer pairs, respectively. Graded interfaces and δ -doping reduce series resistance significantly. Current is injected through the upper Bragg reflector by a full size p-contact. Current confinement is achieved by selective lateral oxidation of a 30 nm thick AlAs layer after mesa etching and stable single-mode emission is enforced by small oxide aperture and weak optical confinement. Polarization can be controlled using off-angled substrate or elliptical current apertures [3]. Mounting the array junction-side down is done straightforward since all electrical contacts are on the top-side

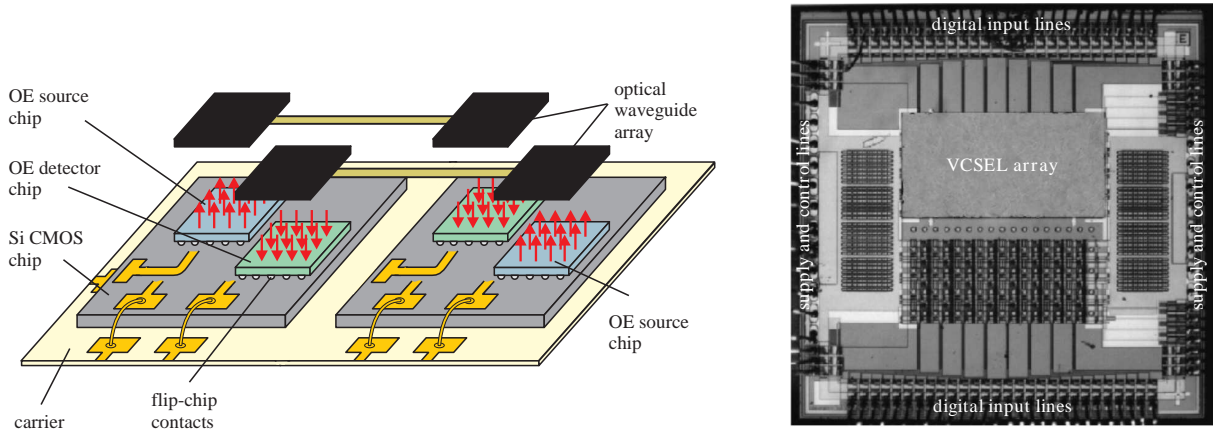


Fig. 1. Schematic of parallel optoelectronic interconnect on chip-level (left-hand side) and 4×8 VCSEL array flip-chip mounted on Si CMOS driver circuits (right-hand side).

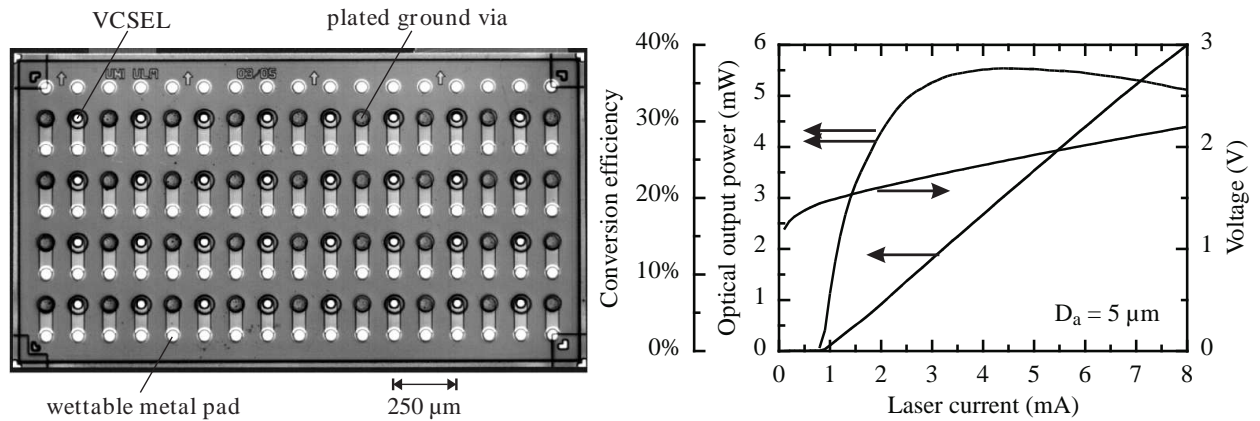


Fig. 2. Photograph of a bottom emitting 4×8 element VCSEL array with 250 μm pitch and two individual contacts per device (left-hand side) and operation characteristics of a 5 μm oxide diameter device within an array (right-hand side).

and laser emission occurs through the substrate at 980 nm wavelength. The layout concept can be carried forward to the optical interconnect standard 850 nm wavelength regime by employing, e.g., GaAs substrate removal after mounting [4]. The VCSELs are arranged at 250 μm pitch and have two contacts per device for individual high bit rate modulation. The VCSELs as well as the plated vias, which connect the n-contact to the top-side metallization, are connected by tracks to remote wettable metal pads.

The right-hand side of Fig. 2 presents driving and output characteristics of an array device with 5 μm active diameter. The threshold current is 0.9 mA and the threshold voltage is 1.45 V. At an optical output of 1 mW the voltage drop across the device is only 1.6 V. The operation characteristics of VCSELs designed to achieve low series resistances and high conversion efficiencies at low output power (e.g. 1 mW) are listed in Tab. 3

As the VCSEL source chips are to be mounted on Si CMOS chips which can get very hot it is important to know about the temperature dependence of the operation characteristics. Fig. 3 shows the variations of threshold currents and laser currents at 1 mW optical output as a function of heatsink temperature of

$D_a = 3 \mu\text{m}$		$D_a = 5 \mu\text{m}$		$D_a = 8.5 \mu\text{m}$	
threshold	$P_{opt}=1 \text{ mW}$	threshold	$P_{opt}=1 \text{ mW}$	threshold	$P_{opt}=1 \text{ mW}$
$I=0.6 \text{ mA}$	$I=1.8 \text{ mA}$	$I=0.9 \text{ mA}$	$I=2.1 \text{ mA}$	$I=1.8 \text{ mA}$	$I=3.1 \text{ mA}$
$U=1.5 \text{ V}$	$U=1.7 \text{ V}$	$U=1.45 \text{ V}$	$U=1.6 \text{ V}$	$U=1.48 \text{ V}$	$U=1.58 \text{ V}$
$\eta_d=65 \%$	$\eta=33 \%$	$\eta_d=64 \%$	$\eta=30 \%$	$\eta_d=62 \%$	$\eta=21 \%$
	$R_d=155 \Omega$		$R_d=107 \Omega$		$R_d=71 \Omega$
$P_{ds}=0.9 \text{ mW}$	$P_{ds}=2.1 \text{ mW}$	$P_{ds}=1.3 \text{ mW}$	$P_{ds}=2.4 \text{ mW}$	$P_{ds}=2.7 \text{ mW}$	$P_{ds}=3.9 \text{ mW}$

Tab. 3. Operation characteristics of VCSELs with different active diameters.

three VCSELs with $5 \mu\text{m}$ active diameter. The In content of the QWs is chosen to obtain a gain peak wavelength of 955 nm at room temperature. At room temperature the cavity mode which determines the emission wavelength and the spectral gain peak of the VCSEL emitting at $\lambda_{rt}=954 \text{ nm}$ is aligned. The VCSELs emitting at $\lambda_{rt}=967 \text{ nm}$ and $\lambda_{rt}=984 \text{ nm}$ have a relative mode-gain misalignment of $+12 \text{ nm}$ and $+29 \text{ nm}$ at room temperature, respectively. The VCSEL with room temperature mode-gain detuning of $+29 \text{ nm}$ (triangles) operates as a temperature insensitive laser as the detuning at room temperature results in mode-gain alignment at a higher temperature. The wavelengths and the differential quantum efficiencies of the VCSELs shift at a rate of 0.07 nm/K and $-0.2 \%/K$, respectively.

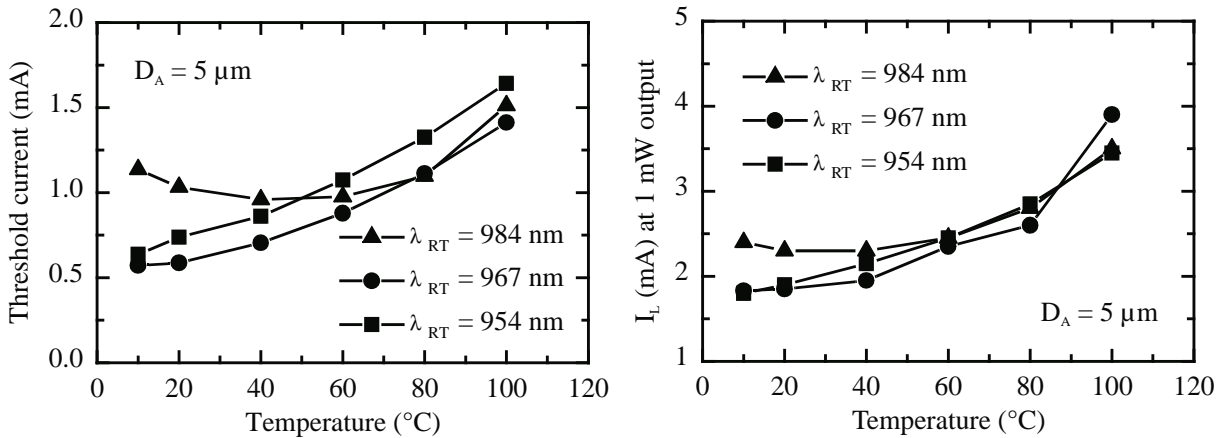


Fig. 3. Variations of threshold currents (left-hand side) and laser currents at 1 mW output power (right-hand side) as functions of heatsink temperature for the three VCSELs with different mode-gain offsets. The active diameter of the VCSELs is about $5 \mu\text{m}$ and the gain peak wavelength at room temperature is about 955 nm .

3. Small Signal and Large Signal Modulation Properties

The left-hand side of Fig. 4 shows the physical origin of an equivalent-circuit model for the VCSEL impedance behavior. The equivalent-circuit model takes into account bond pad capacitance C_{pad} , series resistance R_s , oxide aperture capacitance C_{ox} , and active layer series resistance R_a . Quantities of the various elements are obtained by fitting the model to the measured RF S11 parameters. For the vector high frequency impedance measurements individual lasers from a polyimide planarized 4×8 array are contacted with a coplanar probe tip. The model well describes the measured data up to frequencies of about 20 GHz . Tab. 4 gives determined parameters for three VCSELs of differing active and mesa

diameters. Only R_a depends significantly on the bias current, the value listed here is for a bias current of 3 mA. The parameters scale with the dimensions of the VCSEL and therefore the physical origin proposed above seems reasonable. The solid lines in the right-hand side of Fig.4 depict the bias

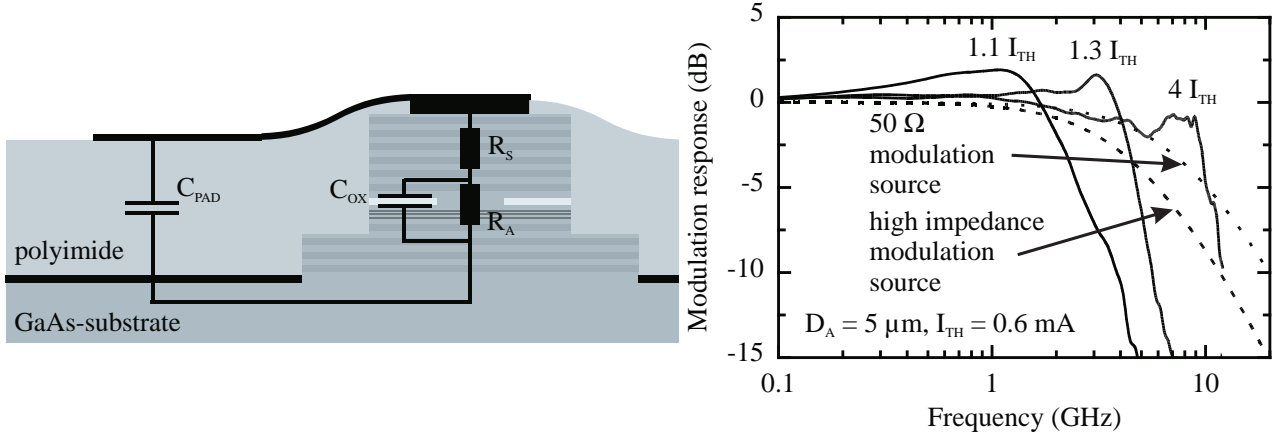


Fig. 4. An equivalent-circuit model for VCSELs (left-hand side) and measured (solid) small-signal modulation response curves of a VCSEL and calculated (dashed) low-pass filter curves for 50Ω and high impedance modulation source (right-hand side).

D_a (μm)	D_m (μm)	R_s (Ω)	R_a (Ω)	C_{ox} (pF)	C_{pad} (pF)
3.5	32	55	100	0.56	0.13
5	34	46	61	0.68	0.13
8.5	38	36	35	1.0	0.13

Tab. 4. Equivalent-circuit parameters obtained by fitting the vector impedance of VCSELs with different active diameters (D_a) and mesa diameters (D_m).

dependent small-signal modulation response curves of a $5 \mu\text{m}$ VCSEL measured with a 50Ω network analyzer. The fitted parameters from the equivalent-circuit model allow the calculation of the parasitic roll-off in the modulation response, also shown as dashed lines in the right-hand side of Fig. 4 for both a high impedance and a 50Ω modulation source. The VCSEL modulation bandwidth is seen to be limited by the electrical parasitics.

The left-hand side of Fig. 5 illustrates the high speed characteristics at low bias currents obtainable from the VCSEL devices of various sizes. The $3 \mu\text{m}$ single-mode device exhibits a modulation current efficiency factor (MCEF) of $10 \text{ GHz}/\sqrt{\text{mA}}$ which decreases for larger diameter devices. We have employed a $3 \mu\text{m}$ VCSEL as transmitter in optical data links. The right-hand side of Fig. 5 shows the eye diagram at 12.5 Gb/s PRBS modulation and the bit error rate (BER) curves for back-to-back transmission and transmission over fibers. The VCSEL is biased at three times threshold and modulated with 1 V_{pp}. We used 100 m graded index multi-mode fiber (MMF) or 1.9 km of $9 \mu\text{m}$ core diameter standard single-mode fiber (SMF). In back-to-back transmission the minimum required power at the pin-InGaAs photodiode is -11 dBm to achieve a bit error rate of 10^{-11} at 12.5 Gb/s. This relatively high power is due to the low sensitivity of the 50Ω pin-receiver used.

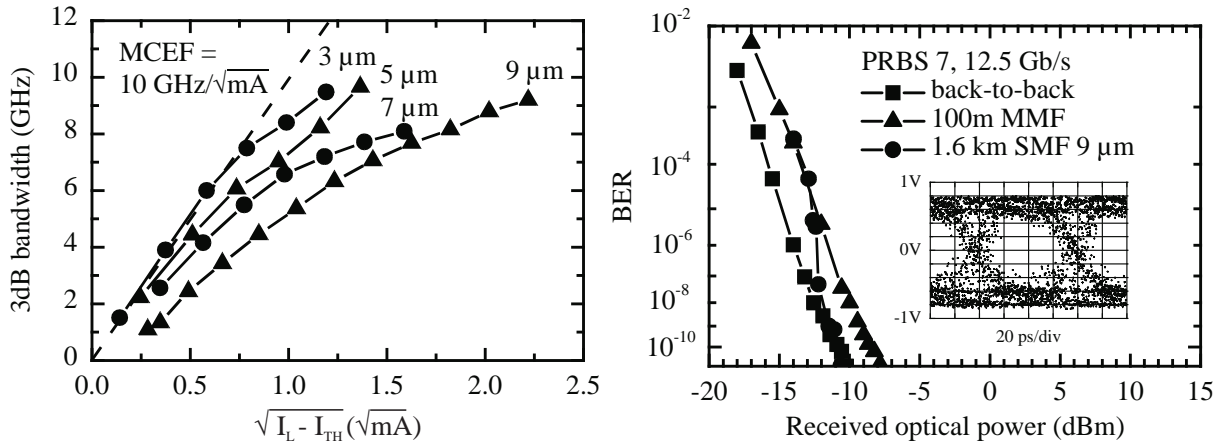


Fig. 5. Bias dependent modulation bandwidths of VCSELs of various sizes (left) and BER curves for different transmission channels using a 980 nm VCSEL with 3 μm active diameter (right).

4. Conclusion

We have designed, fabricated, and characterized selectively oxidized single-mode and multi-mode emitting VCSEL arrays ideally suited as transmitters in chip-level optical interconnects, both in terms of packaging and performance. Single-mode and multi-mode 4×8 VCSEL arrays are flip-chip mounted on Si CMOS driver chips in order to demonstrate VCSEL based optoelectronic transmitters on chip-level. The low-capacitance design of the arrays enables high-speed data transmission up to 12.5 Gb/s per element, far beyond the envisaged Gb/s CMOS speeds.

References

- [1] H. Karstensen et al., in *Proc. 48th ECTC*, pp. 747–754, Seattle, WA, USA, May 1998.
- [2] “<http://www.intec.rug.ac.be/oic>.”
- [3] T. Mukaihara et al., *IEEE J. Sel. Top. Quantum Electron.* **1**, pp. 667–673, 1995.
- [4] K. D. Choquette et al., *Electron. Lett.* **34**, pp. 1404–1405, 1998.