32-VCSEL Channel CMOS-Based Transmitter Module for Gb/s Data Rates

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In the implementation of optical data links, issues of power consumption, bandwidth and sensitivity have to be addressed in the design of optoelectronic components. This is especially important in high density parallel applications where large amounts of heat can cause thermal problems and performance degradation. We present a 0.6 µm-CMOS VCSEL transmitter with 32 data channels whose power consumption is 15.7 mW/ch at 1 Gb/s/ch data transmission.

1. Introduction

The ever increasing CMOS integration density and operation frequency of CMOS chips is causing electrical interconnection bottlenecks to emerge both for inter-chip and intra-chip interconnections. These bottlenecks may turn into serious roadblocks to the continuation of the growth[2] that we have witnessed over the past years. Densely packed, high-frequency electrical interconnects suffer from severe problems: reflections due to impedance mismatch, cross-talk, signal distortion, and electromagnetic interference are difficult to overcome with increasing frequencies and densities. Optical interconnects circumvent these problems and may provide a solution to the interconnect bottleneck.

One of the key components in any parallel optical interconnection system is the array of light sources. In almost all cases one chooses diode-type devices which emit the light beam vertically to the chip, in particular VCSELs. Generally speaking, the most attractive features of VCSELs include on-wafer testing capability, mounting technology familiar from the low-cost light emitting diode market, circularly symmetric beam profiles for ease of light focusing, high-speed modulation with low driving currents, temperature insensitive operation characteristics, and obvious forming of one- or two-dimensional arrays.

To explore the future applicability of direct optical interconnection on a CMOS chip-to-chip level, University of Ulm is serving as partner in a joint European research project named *Optically Interconnected Integrated Circuits* (OIIC)[3] by fabricating the VCSEL arrays [1, 2]. Flip-chip soldering is used to hybridly integrate the optoelectronic chip epitaxial side down with silicon CMOS.

[2]See the Semiconductor Industry Association's (SIA's) *National Technology Roadmap for Semiconductors, 1999 edition*, URL http://public.itrs.net/

[3]See URL http://intec.rug.ac.be/OIIC/

Different demonstrator systems are realized within the OIIC project. Here we report on a 0.6 μm-CMOS VCSEL transmitter with 32 channels which will be used in Gb/s CMOS-to-CMOS link demonstrators.

2. VCSEL Transmitter

On the CMOS driver chip shown in Fig. 1, the main block is a 4×8 array with 16 CMOS data inputs, with the option to use an on-chip pseudo random bit sequence (PRBS) generator. Individually addressable CMOS data inputs are provided to 12 channels in the other two rows of sources. The remaining four source channels are set up with direct access, which allows the verification of the performance of the source components and connections made on flip-chip assembly. For modulation each of the lasers is shunted

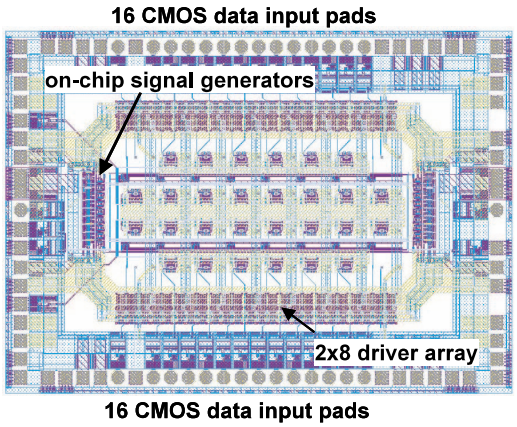

Fig. 1. CMOS VCSEL driver chip designed by ETH Zürich.

with the current I_{DC1} and a switch is used to steal the current I_{DC2}, i.e. the modulation current. It is important that the current taken from the supply is constant, i.e. it does not depend on how many optical channels are turned on or off.

Fig. 2 shows photographs of a fabricated transmitter chip where a bottom-emitting VCSEL array with 4×8 elements has been flip-chip mounted on a 0.6 μm-CMOS driver chip. The bias current of all 28 VCSELs is controlled by a single reference signal. In the left or right hand parts of Fig. 2 all lasers are biased below or above threshold, respectively. The photograph in the center part of Fig. 2 shows the transmitter chip if there is no bias applied to the VCSELs and one of the 16 on-chip PRBS generators is turned on.

Eye diagram measurements are performed by using the on-chip PRBS31 generators, a 3 GHz bandwidth DC-coupled Ge avalanche photodiode and a digital sampling scope. In Fig. 3 measured eye diagrams of 8 VCSEL channels in the first inner row of the transmitter chip at a bit rate of 1 Gb/s are depicted. 28 VCSELs on the chip are biased slightly above threshold and the 16 VCSELs of the inner rows are modulated by the 16 on-chip

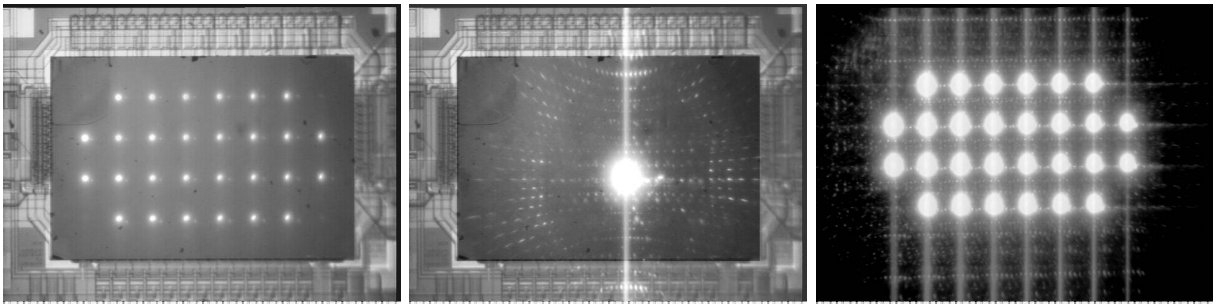

Fig. 2. 0.6 μm-CMOS VCSEL transmitter. The bias current of the 28 channels is controlled by one reference signal and can be set to below (left) or above (right) laser threshold current. VCSELs of the inner two rows can be modulated either by the on-chip PRBS generators (center) or by external CMOS signals.

generators. Good eye opening is observed. The total power consumption of the transmitter chip for these operating conditions is 365 mW resulting in 15.7 mW/ch at 1 Gb/s modulation rate. At 500 Mb/s modulation rate the dissipated power is only 5.9 mW/ch. These results indicate that the developed VCSEL based 0.6 μm-CMOS transmitter has great potential for practical use in implementing high-density and high-speed optical data links at 1 Gb/s/ch.

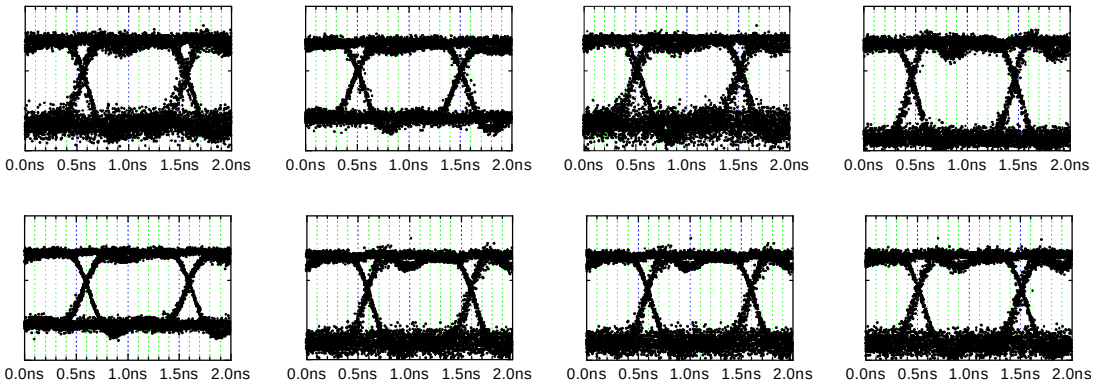

Fig. 3. Eye diagrams of 8 VCSEL-Tx outputs at 1 Gb/s operation speed. The inner 2×8 VCSELs are modulated by the 16 on-chip PRBS31 generators.

3. Conclusion

Apart from single-transmitter modules as for Gigabit Ethernet or one-dimensional parallel links, the much esteemed VCSEL capabilities are most obviously exploited in two-dimensional arrayed systems which can offer massively parallel data transmission and might thus help to avoid the electrical interconnect bottleneck to be expected in future high-performance computer environments.

In this paper, we have reported on a VCSEL based transmitter for high density CMOS-to-CMOS optical interconnection at Gb/s data rates. For the transmitters, two-dimensional VCSEL arrays of 4×8 components on a 250 μm pitch were fabricated. The lasers emit the light at 980 nm wavelength through the substrate or at 850 nm through outcoupling windows in the substrate. The III-V chips are designed for flip-chip bonding to matching pads on the 0.6 μm-CMOS driver chip. On the driver chip the main block is a 4×8 array with 28 CMOS data inputs and the option to use 16 on-chip PRBS generators. The transmitter enables CMOS-to-light signal conversion at 1 Gb/s/ch data rate and power consumption well below 20 mW/ch.

Meanwhile CMOS drivers in 0.25 μm-technology with a special pulse driver circuit are available within the OIIC consortium. A transmitter chip module with drivers in 0.25 μm-CMOS technology – shown in Fig. 4 is under investigation. It is expected to enable data rates exceeding 2.5 Gb/s.

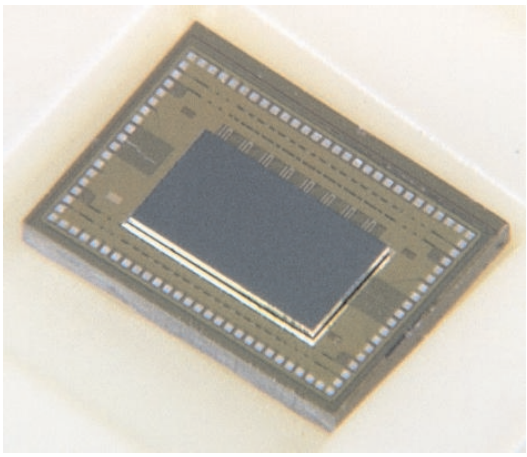

Fig. 4. 0.25 μm-CMOS VCSEL transmitter.

References

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