Flip-Chip Integration of 2-D 850 nm Backside Emitting Vertical Cavity Laser Diode Arrays

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Two-dimensional (2-D) arrays of 850 nm substrate side emitting oxide-confined vertical-cavity lasers are fabricated at a 250 µm pitch. They are designed to provide high frequency modulation capability targeting serial data rates of up to 10 Gbit/s. The arrays are directly hybridized onto silicon fanouts by means of an indium solder bump flip-chip technology. Coplanar transmission lines provided on the fanouts allow for individual addressing of each of the array’s elements. The performance of assembled 8 × 8 laser modules is demonstrated by their basic electro-optical and thermal characteristics.

1. Introduction

While the TMT (Telecommunications, Media and Technology) sectors are severely affected by the current economic slump, bandwidth-hungry applications such as streaming video, e-commerce, and so on still hold the promise of lasting strong profit margins. Therefore, further escalating data traffic levels are predicted. Optical networking will eventually be the only feasible solution to support this continuous growth of data rates well into the future. The increase in throughput of the fiber-equipped long-haul backbones has shifted the bandwidth bottleneck upstream, i.e. deeper into the network. There, in the central offices, the limitations of electrical interconnects create the demand for ultra dense, high data rate, power and cost efficient short-reach optical interconnects between routers and switches in major hubs, and all the way down to the inter-board, inter-chip and even intra-chip levels. Since the component count soars the deeper the penetration into the network is, inexpensive and easily manufactured optical devices are required.

Vertical-cavity surface-emitting lasers (VCSELs), due to their surface-normal light emission, lend themselves to the design of massively parallel optical transmitters implemented as two-dimensional array configurations. Due to their silicon IC compatible low-cost wafer scale manufacturing and testing, VCSELs have the potential to significantly reduce the cost of active optical network components. The circular low divergence output beam shape facilitates light launching to optical interfaces without the need for complicated optics. High power conversion efficiencies complement other integration-friendly properties of high-performance VCSELs and lead to reduced heating in densely packed transceiver modules. In consequence, 2-D VCSEL arrays enable network equipment designers to consolidate and save space, while making their infrastructure as high-performance and cost-efficient as possible.
In this report, 2-D optical high-speed transmit modules for multimode fiber based short haul links are presented. Fabrication details are given and basic characterization of the finished modules is provided in terms of their electrical and optical properties as well as the heat management of the assembly.

2. Device Structure and Fabrication

Oxide-confined VCSEL arrays with backside emission at the standardized 850 nm wavelength are implemented in a flip-chip ready configuration. In a real world application, these would typically be hybridized to an ASIC driver chip performing the required logic functions. In this work, the carrier substrate is a silicon fanout on which low loss coplanar transmission lines serve to separately address the individual devices with high frequency signals. The VCSEL arrays are directly attached to the fanouts by indium solder bump bonding. This technology provides high-speed, high signal integrity (e.g. low parasitics) electrical interfaces potentially supporting serial data rates up to 10 Gbit/s.

2.1 Flip-chip ready VCSEL arrays and the silicon fanout

The schematic cross section of Fig. 1 represents one unit cell of the emitter arrays. The two storied wet etched mesa is the actual laser. It is a generic VCSEL structure made up of three active quantum wells sandwiched between top and bottom Bragg stacks. Lateral current and optical confinement is achieved by selective wet oxidation of a 30 nm thick AlAs film inserted in the first quarter wavelength layer above the p-type cladding of the inner cavity.

Since light emission is through the n-mirror, the current can be injected through a full size Ti/Pt/Au metalization covering the entire contact area of the p-mesa where low mobility hole conduction prevails. Flip-chip bonding requires the n-contact to be fabricated on
the top side as well. Ge/Au/Ni/Au metalization surrounding the mesa ensures a low resistance contact to the highly n-doped 3 μm thick AlGaAs buffer layer through which electrons are laterally fed to the active region. In this flip-chip ready design, n- and p-solder pads are formed at the same elevation, on top of the polyimide passivation. Lateral transmission lines connect these bond pads to their respective VCSEL contacts. This necessitates an additional polyimide non-wettable layer which restricts the solder flow to the circular pads during the subsequent flip-chip bonding process.

Fig. 2: Left: 15 × 15 mm² silicon fanout on which 50 Ω coplanar transmission lines allow separate addressing of the individual devices in the array with high-frequency signals. Right: closeup of the center region showing the solder pad configuration.

The photographs of Fig. 2 show the silicon fanout to which 8 × 8 VCSEL arrays can be hybridized. The 64 coplanar transmission lines of 50 Ω characteristic impedance, defined by standard lithography and lift-off, are used for high-frequency signal transmission. A 250 nm thick intermediate dielectric (SiO₂) on top of the semi-insulating silicon substrate minimizes otherwise noticeable leakage currents. Just like on the VCSEL chip, a polyimide protective coating is applied to most of the subcarrier’s top surface. Its primary function is, however, the confinement of the indium solder to the bond pads during reflow in the center region. Low-loss contacts can be established to the transmission lines around the circumference of the 15 × 15 mm² chip using commercial microwave probe heads. Thick electroplated nickel was used for the bond pads since it is an effective diffusion barrier for the indium solder, and is also well wettable by it. Every 4 of these pads belong to one cell since multiple n-contacts have been implemented in an effort to promote heat transport away from the active device. As is visible in the right part of Fig. 2, there are elbow marks aiding coarse pre-alignment and pads for monitor bumps in every corner.
2.2 Flip-chip joining and final preparation

The indium bumps can be formed on either of the two substrates to be flip-chip joined. Solder deposition by evaporation offers, in contrast to electroplating, better height control as well as the additional degree of freedom to vary the bump sizes, if needed, by utilizing more or less of the area between the bond pads. The bonding process proved to be simple and reliable since, the solder being a pure metal, no alloy related problems like decomposition leading to brittle high resistivity connections can occur.

The pre-alignment of the approximately $2 \times 2 \text{mm}^2$ laser chip to the fanout is done manually by coarsely placing it face down on the bumps and then pushing it to a pre-aligned position under a microscope. During the high-temperature bonding process, the restoring force exerted by the surface tension of the molten solder moves the VCSEL array into a nearly perfectly aligned position. This self-alignment mechanism, which starts working once the indium wets the bond pads, was found to be a useful indicator for the establishment of the bonds. Up to 100% bonding yield is achieved with the method described. Figure 3 displays a VCSEL array bonded to a fanout chip. The state shown is prior to underfill injection, and, therefore, the GaAs substrate is not yet removed.

![Fig. 3: Flip-chip bonded VCSEL array prior to underfill injection and substrate removal. It is aligned to the elbows on the fanout by the restoring force of the molten solder.](image1)

![Fig. 4: Completed 64 channel transmit module. All that remains of the VCSEL wafer is a fragile sheet of epitaxial layers of $3 \mu \text{m}$ thickness, except for the thicker mesas.](image2)

After the two substrates are flip-chip joined, the gap between them is filled with an epoxy adhesive to provide environmental protection and mechanical stability to the module. Reliability is improved this way by reducing the thermal stresses imposed on the solder joints and thus mitigating creep and whisker growth, the two problems frequently associated with indium solder.

For the light generated in the GaAs active region of the bottom-emitting VCSELs to be able to actually escape, the GaAs substrate, which is highly absorptive at the operating wavelength, has to be removed before the module can be put to use. GaAs substrate removal is done successively in the course of the fabrication. The VCSEL wafer...
is pre-thinned down to 200 μm by chemical mechanical polishing before the arrays are singularized and flip-chip bonded. However, the substrate cannot be fully taken off until the module is stabilized by the underfill. The remainder of the substrate is removed with a selective spray etch process that stops at the etch stop layer (ref. to Fig. 1). Finally, this etch stop layer is wet chemically removed. The result, a completed 64-channel transmit module, is presented in Fig. 4. The 2 × 2 mm² VCSEL chip is thinned down to a sheet of only 3 μm thickness. All that remains of the VCSEL wafer are the epitaxial layers. Due to partial transparency, the bottom surface is visible and each 250 × 250 μm² VCSEL cell in the array can be distinguished. The dark frame surrounding the array is the cured underfill.

3. Basic Characteristics

A complete LIV (optical output power, driving current and voltage) characterization was done for all channels of a finished module. The results are shown in Fig. 5. The basic VCSEL performance as well as array homogeneity can be accordingly assessed. Lasing of the 10 μm current aperture devices sets in consistently at 1 mA and 1.8 V. An optical output power of 1 mW is reached at 2.7 mA and 1.9 V. The curves exhibit rather good homogeneity except for the one outlier with substantially enhanced output power for unclear reasons. The shorted VCSEL could well be caused by faulty transmission lines on this particular early fabricated fanout chip.

![Fig. 5: VCSEL cw operation characteristics of all 64 channels of a finished module.](image)

![Fig. 6: Optical spectra of one of the VCSELs at two different operating points.](image)

The exemplary spectra of Fig. 6 at two different operating points as indicated in the graph reveal a pronounced red-shift. It corresponds to a thermal resistance of about 2.6 K/mW. Hence, the devices heat up significantly at higher driving currents. This is partly responsible for the low value of the differential resistance of about 25 Ω. Thermal emission of charge carriers across the heterojunctions in the mirrors account for a large portion of the thermal resistance, which is enhanced at elevated temperatures. However,
higher operating temperatures are in general detrimental to the long-term reliability of the devices.

![Graph](image)

**Fig. 7:** Typical far-field intensity distributions at different operating currents.

Typical far-fields at different operating currents are given in Fig. 7. Owing to the position of the oxide layer within the p-mirror, the mode pattern experiences strong index guiding. As a result, many higher order transverse modes can oscillate simultaneously (as is evident in Fig. 6). The sheet resistance of the n-buffer layer leads to current crowding near the edge of the oxide aperture. This enhances the effect of spatial hole burning and favors those higher order modes as they better overlap with the lateral gain profile. They therefore take over at higher currents. The result is a donut-like intensity distribution particularly at higher currents which, in conjunction with a relatively large divergence angle of about 25° (FWHM), complicates light coupling to fibers.

4. Conclusion

64-channel optical transmit modules were successfully fabricated by hybridizing 8 x 8 VCSEL arrays to fanout chips employing an indium solder bump flip-chip bonding technology. While quite favorable cw operation characteristics of great consistency throughout the arrays were obtained, small signal modulation along with data transmission remain to be examined. A thermally optimized VCSEL design is to be implemented aiming at significantly lower thermal resistance values. Furthermore, work also has to be done to reduce the divergence angle of the donut-shaped far-field.

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