Self-Separation of GaN Using In-Situ Deposited SiN as Separation Layer

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Thick, self-separated GaN layers have been grown by hydride vapor phase epitaxy (HVPE) on templates with SiN-interlayers, which worked as the separation layer. The used templates were prepared by metalorganic vapor phase epitaxy (MOVPE) to start with an excellent seed layer. As several groups reported, it was observed, that by using only one SiN-interlayer, the dislocation density could be reduced by an order of magnitude. To use the SiN-interlayer as separation layer, a much weaker connection between the template and the thick HVPE grown GaN should be generated. To study the separation process in-depth, we started our studies with a stack of multiple SiN-interlayers. Those structures lead to large masked areas or even, by the right choice of the deposition parameters, to a cavernous layer. On those templates, the separation during the cool down of nearly full 2 inch wafers could be observed. These thick self-separated HVPE layers showed a smooth surface morphology with excellent optical and electrical properties.

1. Introduction

The improvement of GaN based electronic and optoelectronic devices is still limited by the fact that epitaxial structures, like lasers and LEDs, have to be grown on foreign substrates like sapphire or SiC, because high quality GaN-wafers are not yet really available for an adequate price. The growth on such foreign substrates causes a high defect density, which limits the device performance. It has been estimated that the dislocation density should be below $10^6\,\mathrm{cm}^{-2}$ in order to get high lifetime and a good radiative efficiency for LASER structures. Many groups investigated techniques like, e.g., laterally epitaxially overgrown GaN stripes to reduce the defect density [1]. Although, those groups could control the propagation and the arrangement of the threading dislocation, they could not reduce the dislocation density homogenously over the whole wafer. To get homogenous, low dislocation densities, it is essential to do homepitaxial growth of GaN. To generate such substrates for the homoepitaxial growth, the growth of thick layers by hydride vapor phase epitaxy was developed by several groups. Excellent optical devices could be fabricated on such HVPE grown quasi-substrates, but these non-freestanding substrates still suffer from several problems. The used foreign substrate for thick GaN make backside contact difficult or even, in case of sapphire, impossible. Moreover, the strain induced by the foreign substrate results in strong bending of these non-freestanding quasi-substrates.

To overcome these problems, freestanding GaN-wafers have been prepared by removing the foreign substrate after the HVPE process. In most cases, this requires some complex, time consuming processes like laser lift-off [2] or special substrates like GaAs, which can be removed by wet chemical etching [3]. Another possibility is the self-separation of the GaN-layer from the substrate during cool down, using the difference in thermal expansion coefficients. For the self-separation process, it is necessary to define the breakpoint between the substrate and the thick grown GaN-layer. This can be defined with different methods. It is possible to generate the breakpoint with a TiN layer which leads to a cavernous layer [4]. The deposition of a dielectric mask, as it is used for epitaxial lateral overgrowth could also lead to a perforated layer between the substrate and the thick GaN-layer [5]. All of these methods require additional ex-situ steps for preparing the freestanding GaN-substrate. Therefore we focused our studies on a self-separation process during cool down. To avoid additional ex-situ steps, we generate the perforated layer with in-situ deposited SiN-interlayers.

2. Experimental

The HVPE growth experiments have been performed in a commercial single wafer HVPE machine with horizontal quartz reactor. As usual, metallic Ga was transported by HCl gas to the substrate, whereas ammonia was used as nitrogen precursor. The Ga source was kept at 850°C, while the substrate zone was heated to 1010–1070°C. A freely adjustable mixture of N_2 and H_2 could be used as carrier gas to control the strain during growth. The reactor pressure was mostly kept around atmospheric pressure, to achieve a high growth rate.

By growing on quarters of 2 inch templates, up to 4 different templates could be overgrown simultaneously in one HVPE growth experiment, to get a fair comparison between the templates. The templates were grown on (0001) sapphire substrates in a AIXTRON 200/4 RF-S MOVPE system. Trimethylgallium, trimethylaluminium, ammonia and diluted silane were used as precursors for the template growth. The growth parameters were close to parameters for standard GaN growth in MOVPE. To achieve a smooth surface after the HVPE growth, all experiments have been carried out on slightly misoriented sapphire substrates [6]. The sapphire was first heated to 1200°C for thermal cleaning, afterward an AlN nucleation layer was deposited at 900°C. Finally, a thin GaN layer covers the nucleation layer, before the SiN-interlayers were deposited. To study the influence of the SiN-layers on the HVPE growth and the self-separation, the stack of SiN- and GaN-layer was varied to increase the separation probability.

3. Results and Discussion

3.1 MOVPE growth of SiN-layers

We started the investigation of the interlayers with the deposition of single SiN layers. First we studied the influence of reactor pressure, total flow, temperature and ammonia supply. The best deposition conditions could be achieved with a reactor pressure of 100 mbar, around 1100°C with a low ammonia supply, compared to standard GaN growth conditions. Our experiments exhibited, that the temperature mainly influences the deposition rate of the SiN-interlayer [7]. Therefore, we controlled the thickness of the interlayer by the deposition time and kept the temperature constant. By using one SiN-interlayer, Fang et al. [8] reported a significant defect reduction. Our studies of single SiN-interlayer confirmed those results. We got a decrease in dislocation density with increasing SiN layer thickness. We estimated the dislocation density to a value of $2 \cdot 10^8\,\mathrm{cm}^{-2}$ with a deposition time of 6 min. Longer deposition times results in a rough and non coalesced surface morphology with a masked area on the bottom of a pit. The defect density was evaluated from atomic force micrographs were the dislocations were marked by chemical etching [9].

The SiN-coverage was estimated from the silicon incorporation in a n-doped layer grown with the same process parameters, by calculating the amount of silicon for one complete SiN monolayer. In addition, the coverage could be estimated from pictures of an optical or scanning electron microscope (Fig. 2). This is done by the measurement of the area of small pyramids grown after the SiN-interlayer divided by the hole area of the picture. These measurements confirmed the calculated values for the SiN-coverage.

The most important property of the separation layer is to generate a weak connection between the template and the the thick GaN-layer, as it is the case for TiN- or low temperature interlayers [10]. The second task is to admit an HVPE growth on top. Both major tasks are achievable by using SiN. As mentioned above, by increasing the SiN deposition time, we could achieve a higher coverage with non overgrown areas in MOVPE. However, we observed a bad separation by only increasing the thickness of one SiN-interlayer. To overcome the problems with only one interlayer, we started the deposition of multiple, low coverage SiN-layers with a short GaN growth in between (Fig. 1). The sample in those figures consist of six periods of SiN and GaN. To improve the lateral overgrowth, we doped the layers slightly with magnesium [11].

The use of multiple SiN interlayers leads to several effects. On the one hand, in Fig. 1, it is clearly seen, that overgrown holes developed, which leads to a visible disconnection. A comparable structure was achieved by Y. Oshima et al. [4] using a TiN interlayer for their separation process. This could be achieved by using a relatively low SiN coverage per layer. On the other hand, by increased coverage per layer of a factor of 1.5, the structure of the SiN-template changed completely (Fig. 2). Large areas of the surface are covered with SiN. The increased SiN deposition time causes a coverage of small pyramids and the base of larger pyramids. The distance of those larger pyramids is in the range of 4 µm. This is also suitable for the HVPE overgrowth.

3.2 HVPE growth on templates with SiN-layers

As mentioned above, up to four quarter wafers could be overgrown at the same time, to achieve the best comparability between different templates. We started with the growth of up to 120 µm thick layers on sapphire templates without cracks [12]. By the optimization of the process parameters, we could achieve a mirror like surface morphology [13]. With a further increase of layer thickness on bare templates, the cracking probability increases in the same way. Those cracks, that destroyed the samples, developed only during the

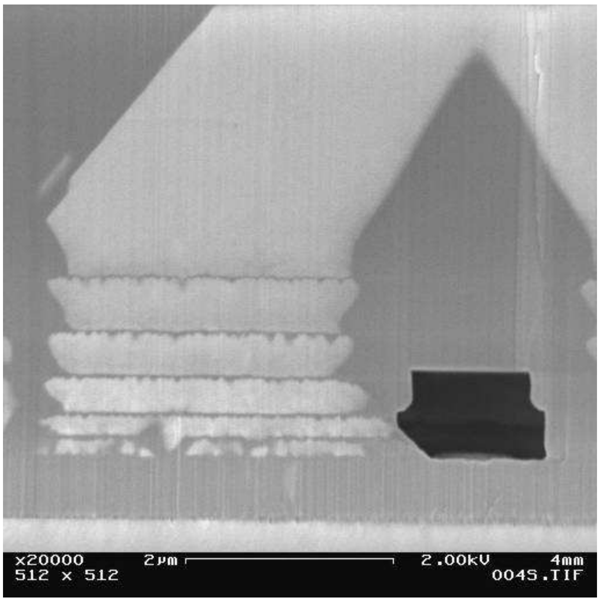

Fig. 1: SEM picture of the cross section of a sample with SiN-interlayers. Six SiN-interlayers are visible and form a cavernous layer, where the separation occured.

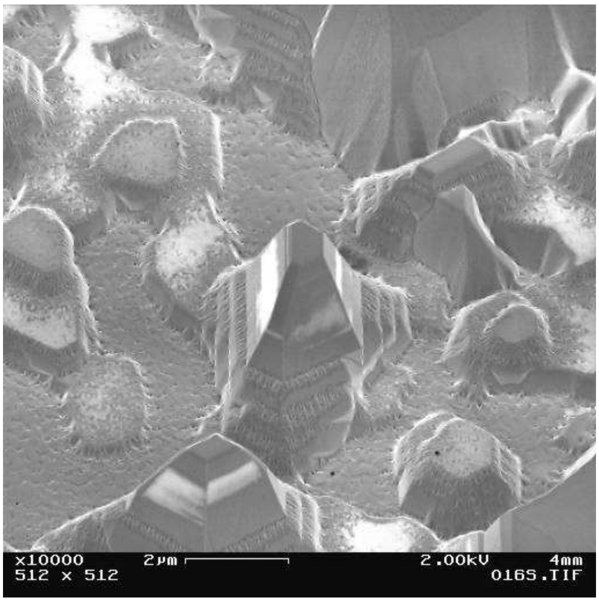

Fig. 2: SEM picture of the surface of a template with a higher SiN-coverage as in Fig. 1. The increased SiN-coverage leads to freestanding pyramids with large masked areas in between.

cool down, induced by the difference in the thermal expansion coefficients of sapphire and GaN.

These results show that the used parameters are suitable for the growth of thick layers. Moreover, we observed that SiN-interlayers lead to a significantly decreased cracking probability in thick GaN layers. This indicates that the SiN-interlayer influences the strain in the same way as it is the case on laterally overgrown templates.

With a layer thickness of approximately 300 µm, the first small area delamination processes were observed. The analysis of those separated small pieces exhibited, that the cracks propagate in the separation layer. Due to a strong connection between the substrate and the HVPE layer and the relatively low thickness of the HVPE layer, also vertical cracks developed. Hence, it is necessary to grow thick GaN-layers and reduce the bonding strength of the separation layer. First we increased the thickness of the layers to improve their stability for the separation process. Large self-separated freestanding samples wit a size of 15x25 mm, could be achieved with a HVPE grown thickness of 600 µm. By a further optimization of the growth parameters, we were able to grow 1.2 mm thick layers with a growth rate of approx. 250 µm/h. This increase of layer thickness tends to result in the separation of large freestanding samples (Fig. 3).

The rough backside, which can be seen in the picture, is caused by the separation layer. Also a high density of inverse pyramids is visible, which causes a change in the surface smoothness around the pyramids. This is also the reason for the incomplete separation of the 2 inch wafer. The crack occurs near the highest density of inverse pyramids (Fig.

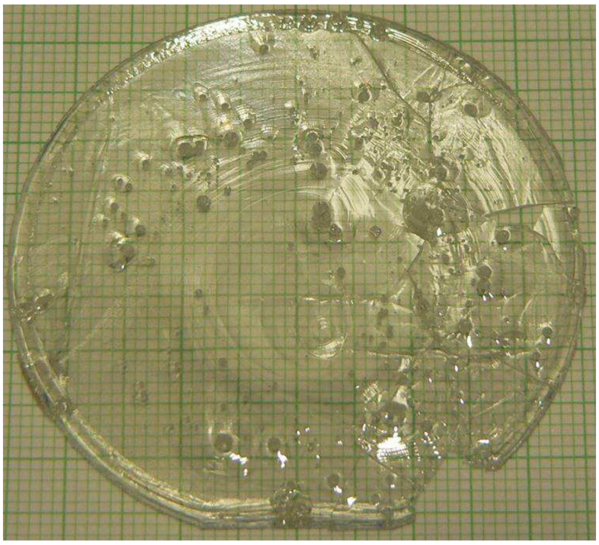

Fig. 3: Nearly full 2 inch self-separated wafer with a thickness of approximately 1 mm.

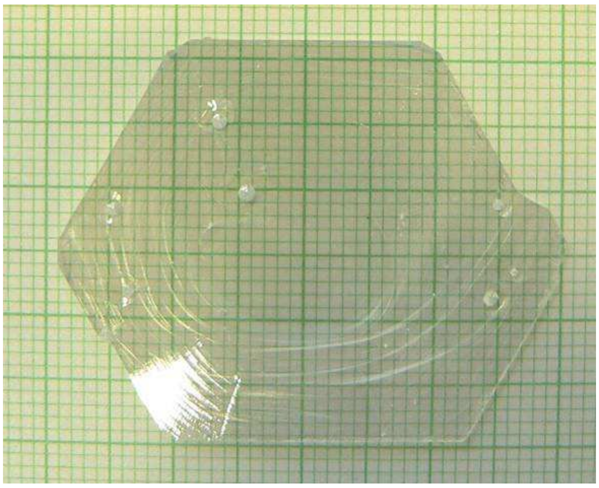

Fig. 4: Sample with a reduced pit density.

3). Parasitic depositions caused a change in diameter of the gas-inlet of the GaCl. This results in a reduced growth rate and a inhomogeneous thickness. Nevertheless, it was possible to separate more than 10 cm^2 out of the center of the sample with the largest thickness. This area is equivalent to a half 2 inch wafer (Fig. 4). We assume, that the lower pit density is caused by the lower growth rate.

In spite of the high growth rate and the partly high inverse pit density, excellent electrical and optical properties could be measured. On the 600 µm thick freestanding sample we found Hall mobilities up to 820 cm^2/Vs with a carrier concentration of approx. $1 \cdot 10^{16}\,cm^{-3}$ at room temperature measured and 3646 cm^2/Vs and $3.6 \cdot 10^{15}\,cm^{-3}$ at 85 K. The surface flatness of the freestanding samples is comparable to high quality MOVPE grown GaN layers, thus enabling the use of these samples for subsequent epitaxial steps without the need of surface polishing.

4. Conclusion

It was demonstrated that a single SiN-interlayer reduces the defect density by an order of magnitude. By further increase of the deposition time, non overgrown masked areas developed. By using those interlayers in a periodic stack, it was possible to generate a cavernous layer or larger masked areas with singe pyramids - both structures lead to a separation. The growth of a 1.2 mm thick layer on such a template resulted in almost 2 inch self-separated wafers. They exhibited excellent optical and electrical characteristics.

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