Investigations into Matrix-Addressable VCSEL Arrays

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We report on fabrication and characterization of densely packed top-emitting 16×16 *elements wire-bonded matrix-addressable vertical-cavity surface-emitting laser (VCSEL) arrays, which may find future applications such as non-mechanical particle movement with optical multi-tweezers, confocal microscopy or free-space communications with beam steering capability. The factors that control packing density such as layer structure, mask design and VCSEL processing are investigated aiming to minimize the pitch between VCSELs in the array.*

1. Introduction

The impressive performance of VCSELs such as low power consumption, circular beam output perpendicular to the wafer surface, on-wafer testing before packaging, and efficient high-frequency modulation is providing the motivation for a continued search for new device types. Besides, VCSELs are ideally suited to form two-dimensional arrays of compact optical sources owing to their low threshold currents and high packing density. Such two-dimensional VCSEL arrays are attractive for display technology [1], [2], optical scanners [3], optical interconnects and confocal microscopy. All of these applications require convenient addressing of VCSELs in these arrays. In order to allow operation with high packing density, it is important to decrease the number of contact pads required to address the elements in the array. Figure 1 shows how the elements in 4×4 two- dimensional arrays can be addressed using two different architectures. It becomes clear that individual addressing requires a lot of metallic traces. This increases the connection complexity and limits the packing density compared with the matrix addressing scheme. Matrix addressing [4] has the advantage of requiring only $M + N$ contact pads for an $M \times N$ element array, unlike its individually addressable counterpart, which requires $M \times N$ contacts. In addition, when such arrays are monolithically integrated with resonant-cavity photodetectors [5], this will enable a variety of applications such as high-density interconnects, position sensors, and imaging devices. A recent trend in VCSEL arrays is to obtain a coherent laser emission by utilizing photonic crystal VCSELs [6]– [10] as a way to increase the emitted power from a single transverse mode.

This article is organized as follows: In Sect. 2, the layer structure needed to fabricate the laser elements in the array is described. In Sect. 3, the processing is explained and discussed. In Sect. 4, the laser characteristics are evaluated. Finally conclusions are made in Sect. 5.

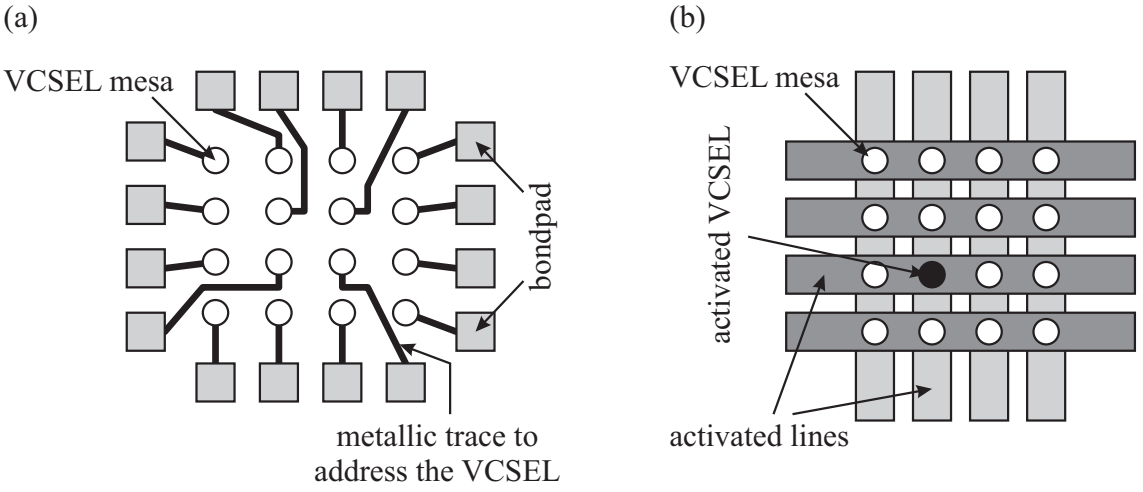

Fig. 1: Sketches of 4×4 VCSEL arrays with (a) independent addressing and (b) matrix addressing schemes.

2. Layer Structure

In order to fabricate matrix-addressable VCSEL arrays, there are some differences in the layer structure compared with common n-contact arrays. For instance, in matrix-addressable arrays the epitaxial structure is grown on an undoped GaAs substrate to allow electrical isolation of columns, in contrast to the common n-contact scheme, which requires an n-doped GaAs substrate. Above the undoped GaAs substrate, there is a 2.5 µm thick heavily n-doped GaAs layer to allow n-metallization. The n- and p-type distributed Bragg reflectors (DBRs) consist of 38.5 Si-doped $Al_{0.2}Ga_{0.8}As/Al_{0.9}Ga_{0.1}As$ DBR pairs and 23 C-doped $Al_{0.2}Ga_{0.8}As/Al_{0.9}Ga_{0.1}As$ pairs, respectively. The DBRs are graded in composition and doping concentration for minimizing the free-carrier absorption and decreasing the electrical resistance. The active region composed of three 7.9 nm thick GaAs quantum wells (QWs) separated by 9.9 nm thick $Al_{0.27}Ga_{0.73}As$ barriers is positioned in an optical cavity with a thickness of one material wavelength. The laser emission wavelength using these materials together with the cavity design is in the vicinity of 850 nm. A 32 nm thick AlAs oxidation layer is placed above the QWs. The function of this layer is twofold: When a part of it is oxidized to form the active aperture, not only the excitation current is confined but also optical guiding of the laser radiation occurs.

3. Fabrication Processes

Firstly, the VCSEL mesas have been defined by photolithography followed by reactive ion etching (RIE). In order to obtain a high packing density it is not possible to use wet-chemical etching, because the mesa side walls will not be vertical but instead have a slope. In addition, wet etching causes an undercut of the AlAs layer for long etching times, as indicated in the scanning electron micrograph in Fig. 2 (left). This is due to the higher etching rate of this layer compared with that of GaAs/AlGaAs. Such an undercut causes stress in the layer structure and makes planarization difficult. For these reasons, RIE has

been utilized. Figure 2 (right) shows a scanning electron micrograph of the RIE- etched mesa. A radio frequency power of 35 W has been used and the gas pressure was 9 mTorr. $SiCl_4$ and Ar with gas flow rates of 10 sccm and 6 sccm, respectively have been employed. Etching was done down to the depth of the n-buffer layer. Amongst the most challenging processes in two-dimensional VCSEL arrays is the separation of columns. The distance between these columns can be as small as 5 µm and the photolithography resolution is not sufficient for the topology resulting from the first etching process. For this reason two different pitches have been chosen to guarantee the success of processing. The fabrication was successful when the separation between columns was 12 µm instead of 5 µm. After column isolation had been carried out, n-metallization was applied on the buffer layer. In order to planarize the etched regions, four polyimide planarization steps were made to allow evaporation of p-metallization through the rows. After this, an 800 nm thick Ni/Au metallic layer was evaporated to serve as bondpads for wire bonding in an integrated chip package. To allow higher packing density, alternating bondpads have been utilized on all sides of the chip. Figure 3 shows a scanning laser microscope top view of a fabricated VCSEL array after wire bonding. A photo of the packaged chip is displayed in Fig. 4

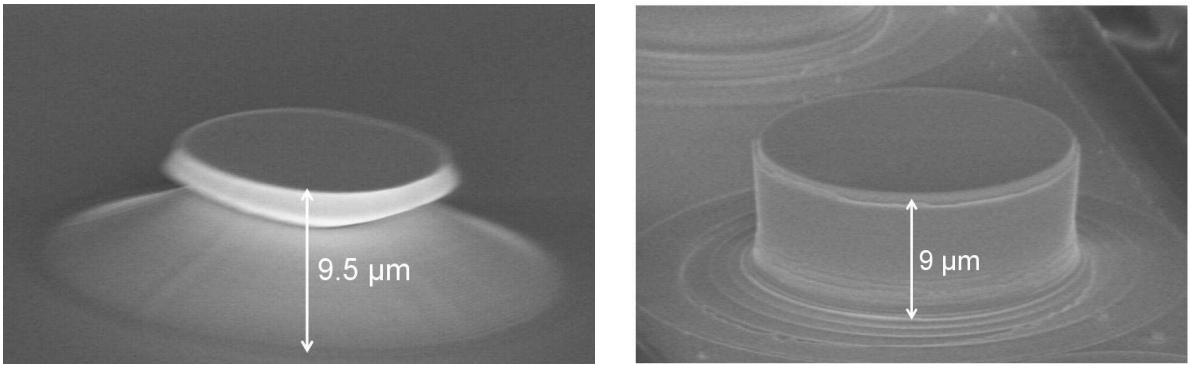

Fig. 2: Scanning electron micrographs of an etched mesa using wet-chemical etching (left) and reactive ion etching (right).

4. Laser Characteristics of Matrix-Addressable VCSEL Arrays

The light–current–voltage (LIV) characteristics of some devices in a fully processed 16×16 elements VCSEL array are displayed in Fig. 5. The distance between centers of two neighboring VCSELs is 84 µm. The active diameter of the aperture is 10 µm. The threshold current varies from 0.5 mA to 1.6 mA and the maximum output power at thermal rollover is between 2.4 and 4 mW. Such variation is due to a gradient in layer thicknesses during crystal growth by molecular beam epitaxy which causes variations in the reflectivities of n- and p-type DBRs and the gain throughout the wafer. The difference in voltage drop from one VCSEL to another is due to a change in the parasitic resistance, namely the longer is the distance from the bondpad to the VCSEL, the higher is the corresponding resistance. A simple analysis of this resistance has been done, based on measuring the resistances of the p-row, n-column and the mesa separately. These individual components

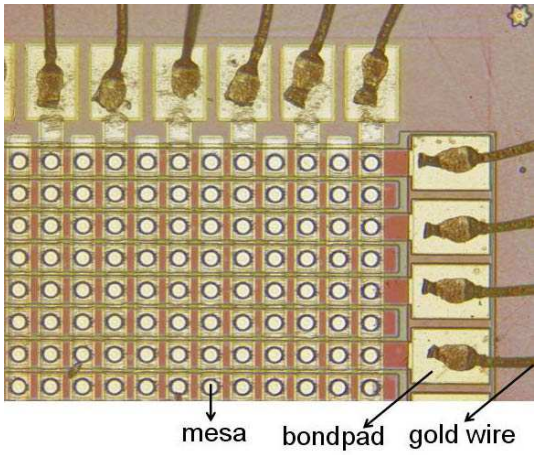

Fig. 3: Scanning laser micrograph of part of a 16 × 16 elements matrix-addressable VCSEL array.

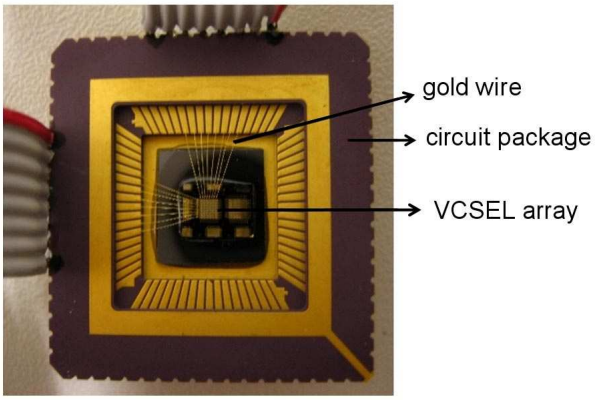

Fig. 4: Photograph of the processed VCSEL array.

were summed up (since the resistors are connected in series) and compared to the resistances extracted from the current–voltage curves. From the measurements, the average p-row resistance is 22 Ω and the n-column resistance is 27.5 Ω. In this analysis, the mesa resistance is assumed to be the resistance of the VCSEL when the nearest electrodes are activated. This resistance varies throughout the wafer due to different etch depths caused by the gradient in layer thickness. Table 1 summarizes the resistances for different mesas.

5. Conclusion

In this article, fabrication and characterization of densely packed (84 µm pitch) top-emitting 16 × 16 elements matrix-addressable VCSEL arrays have been reported. A simple analysis of the parasitic line resistances has been made.

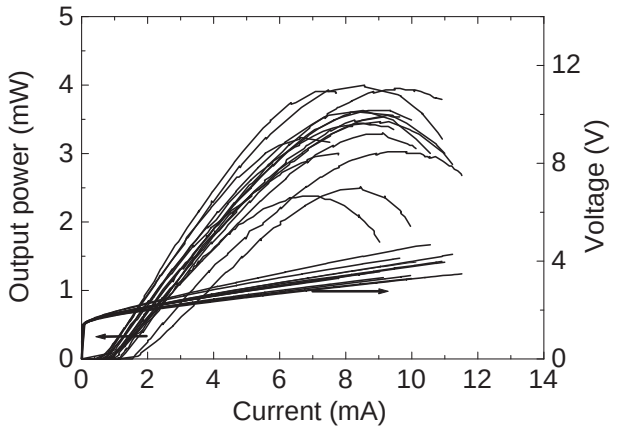

Fig. 5: Light–current–voltage characteristics of some devices within a processed matrix-addressable VCSEL array.

Table 1: Resistances extracted from the IV curves and accumulated measured resistances at different positions within the VCSEL array, where the mesa resistance varies.

Resistance from IV curve (Ω)	Accumulated resistance (Ω)	Mesa resistance (Ω)
174	178	128
153	154	104
144	146	97
138	142	93

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