VCSEL–PIN Transceiver Chips for Bidirectional Gbit/s Data Communication Over Multimode Fiber

Alexander Kern

We present the fabrication and characterization of monolithically integrated transceiver chips with vertical-cavity surface-emitting lasers (VCSELs) and PIN photodetectors for bidirectional optical data communication at 850 nm wavelength over a single butt-coupled standard multimode fiber. With such a low-cost transmission configuration, data rates of 9 Gbit/s in back-to-back mode and 7 Gbit/s over a 500 m long 50 µm core diameter fiber are well possible.

1. Introduction

True bidirectional multimode fiber (MMF) transmission using monolithically integrated transceiver (TRx) chips is one possible way to satisfy the demand for increasingly compact and low-priced high-speed optical interconnection in local-area networks, the industrial or automotive sector. A worthwhile attempt to use a VCSEL as an efficient laser source and a resonant-cavity-enhanced photodetector is introduced in [1]. Such a dual-purpose device is switched between two operation modes. Half-duplex operation at 1.25 Gbit/s data rate over a 50 µm core diameter MMF with 500 m length was demonstrated. Full-duplex data transmission is only possible with spatially separated devices. Unfortunately this solution is not well suited for low-cost links owing to resonant detection, giving very little room for detuning and thus requiring temperature control at both fiber ends. Non-resonant detection is achieved with separate epitaxial layers for photodiode (PD) and VCSEL [2, 3].

In previous work [4] we have studied the transmission performance of TRx chips containing VCSELs and metal–semiconductor–metal (MSM) detectors matched to 200 µm diameter polymer-clad silica (PCS) step-index fibers. Later, the VCSEL–MSM chips were miniaturized for 100 µm core diameter graded-index (GI) MMFs in order to increase the fiber length through a higher bandwidth–distance product. Up to 2.5 Gbit/s full-duplex operation over 50 m fiber were thus demonstrated [5].

Here, for the first time, PIN-type PDs are used in miniaturized VCSEL-based 850 nm-range transceivers for bidirectional optical interconnects via a single, two-side butt-coupled standard MMF, as shown in Fig. 1. The monolithic integration of both components as well as a design avoiding the use of external optics saves space, weight and module cost. To our knowledge, the data rates demonstrated in this paper are the highest reported so far. In addition, our chips do not require temperature control and are suited for full-duplex operation.

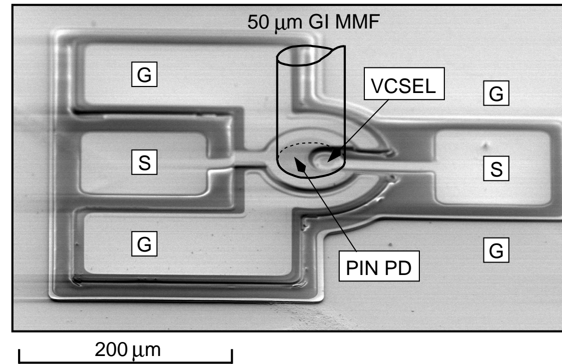

Fig. 1: Scanning electron micrograph of a monolithically integrated VCSEL and PIN PD device. A GI MMF butt-coupled to the transceiver chip is schematically indicated.

2. Transceiver Chip Design and Fabrication

In the full-monolithic chip, the layers for the PIN PD are grown on top of the VCSEL layers in the same epitaxial run using molecular beam epitaxy on GaAs substrates. An up to 3 µm thick undoped GaAs absorption layer is sandwiched between p- and n-doped $Al_{0.3}Ga_{0.7}As$. The higher bandgap energy of these two contact layers provides a spectral window for the wavelengths of interest at around 850 nm. In order to minimize the energy band discontinuities between the absorption and contact layers, linearly graded n- and p-$Al_xGa_{1-x}As$ ($x = 0 \rightarrow 0.3$) is employed, ensuring an easier escape of the light-induced carriers from the undoped GaAs.

A 150 nm thick intrinsic $Al_{0.9}Ga_{0.1}As$ etch stop layer separates the detector layers from the VCSEL and partially acts as an insulator by reducing capacitive coupling between the two devices. The resonator of the VCSEL is built by an n-type doped bottom Bragg mirror grown on an n-doped GaAs substrate and equivalent p-type top mirror pairs. The inner cavity has an optical thickness of one wavelength and contains three 8 nm thick GaAs quantum wells. A 32 nm thick p-doped AlAs layer in the first top mirror pair above the active region is designated for current confinement after an oxidation step. The VCSEL growth is terminated with a 30 nm highly p-doped GaAs layer, which provides a low resistance p-contact and at the same time prevents oxidation of the subjacent aluminum-containing layers.

Eight lithographic steps are necessary for processing the transceiver chip shown in Fig. 2. In the first step, the detector layers on top of the VCSEL are removed by a combination of two reactive-ion etching (RIE) and two wet-etching processes. The uppermost VCSEL layer is not affected by the etching, since it is protected by an etch stop layer with a high aluminum content, as mentioned above. Dry-etching with $SF_6/SiCl_4$ for high etching selectivity between GaAs and $Al_xGa_{1-x}As$ [6] terminates on the 200 nm thick p-doped $Al_{0.3}Ga_{0.7}As$ layer. Wet-etching with a citric acid/H_2O_2 solution ensures sufficient selectivity between $Al_xGa_{1-x}As$ layers with 30 % and 90 % aluminum content [7]. Followed by a selective wet-etching of $Al_{0.9}Ga_{0.1}As$ with hydrofluoric acid, the highly p-doped GaAs cap layer of the VCSEL can now be exposed.

PIN PDs have vertically displaced contacts and thus require an additional etch step to

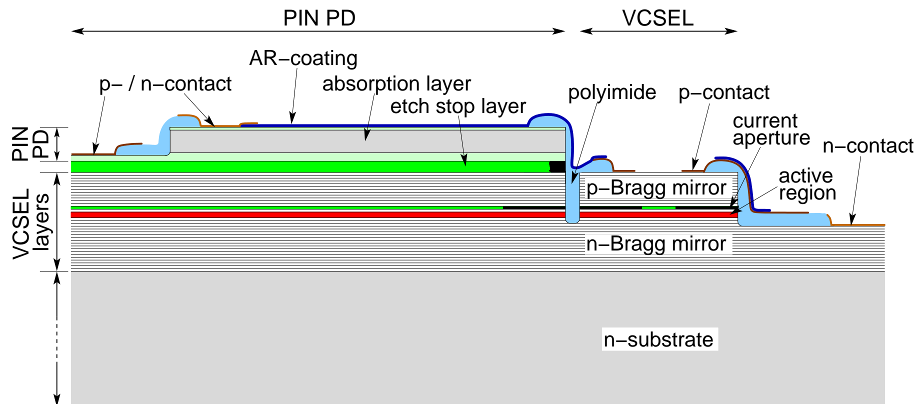

Fig. 2: Schematic cross-sectional view of the fully processed transceiver chip.

expose the p-doped $Al_{0.3}Ga_{0.7}As$ contact layer, as can be seen in the left part of Fig. 2. This step can be accomplished in analogy to the previous dry-etching processes. By means of the described selective etching techniques, a uniform layer topography all over the wafer can be guaranteed in spite of a layer thickness inhomogeneity from epitaxial growth. The third etching process spatially separates the VCSEL and the photodetector by a 2 to 4 μm narrow trench and gives access to the current confinement layer, as seen in the right part of Fig. 2. It is performed just with $SiCl_4$ without selectivity. Also this process step requires reactive-ion etching, since steep mesa side walls are crucial for the miniaturization and dense integration of VCSEL and PIN PD. Selective oxidation in a hot water vapor atmosphere forms the current aperture in the AlAs layer. The fourth and fifth lithography steps provide planarization and passivation with polyimide. Afterwards, both, p- and n-contacts of the PD and VCSEL are evaporated and annealed in order to form low-resistance contacts. In the last lithography step, an Al_2O_3 quarter-wave antireflection (AR) layer is sputtered on the area of the transceiver chip which is exposed to incident light. The reflectivity of the semiconductor surface is thus reduced from approximately 30 % to 1.3 % over a spectral width of nearly 50 nm [5].

3. Device Characteristics

The VCSEL structure underneath the PIN PD leads to back-reflection of the incident non-absorbed light and thus to double-pass absorption. The responsivity of a transceiver PD with 3 μm thick GaAs absorption layer reaches 0.61 A/W at 850 nm, which corresponds to a quantum efficiency of nearly 88 %. For high-speed measurements, both, VCSEL and PIN PD can be contacted directly on wafer by two coplanar microwave probes with a ground–signal–ground (GSG) configuration, as indicated in Fig. 1. The small-signal modulation responses of the PIN PDs are determined by means of a reference laser diode with 7 GHz cut-off frequency which is driven by a constant current superimposed with a low-power RF modulating signal generated by a sweep oscillator. The laser beam is focused via free-space optics on the transceiver PIN PD. The PD under test is biased with a constant voltage, where a bias-tee separates the RF and DC current signals. According to the frequency response in Fig. 3 (left), the bandwidth of a 3 μm thick, 60 μm diameter PIN

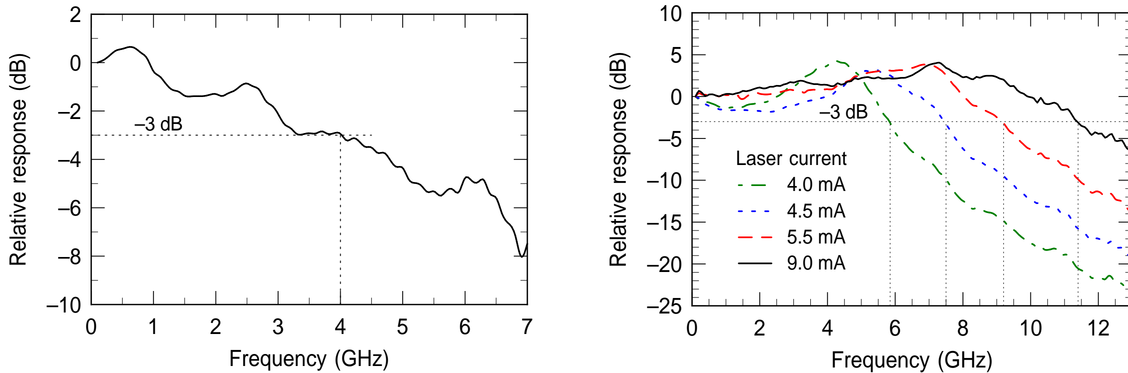

Fig. 3: Small-signal frequency responses of an integrated 3 µm thick transceiver PIN photodiode with a 3 dB-bandwidth of 4 GHz (left) and a typical transceiver VCSEL with a maximum 3 dB-bandwidth of approximately 11.5 GHz (right).

PD is limited to 4 GHz. The resistor–capacitor (RC) low-pass and drift time bandwidths are expected to be about 14 GHz (for $R = 50\,\Omega$) and 15 GHz, respectively. We attribute the much smaller experimental value to parasitic coupling with the highly doped VCSEL layers. Both, the responsivity and the 3 dB-bandwidth of the PD is almost independent of the bias voltage.

The experimental setup for VCSEL small-signal characterization is very similar to the one of the PIN PD. Here, a fiber-coupled reference PD with 25 GHz cut-off frequency is used, where the VCSEL under test is contacted on chip via a GSG microprobe. An RF attenuator between bias-tee and sweep oscillator is used to attenuate the backward microwave reflections due to impedance mismatch between the VCSEL and the $50\,\Omega$ measurement system. A typical frequency response of an integrated VCSEL with about 8 µm oxide aperture diameter is shown in Fig. 3 (right). A maximum 3 dB-bandwidth of 11.5 GHz is observed for an operating current of 9 mA. With a threshold current of 3.5 mA, a maximum output power of 3.5 mW, and optical emission at around 810 nm, there is much room for further optimization.

4. Digital Data Transmission

The small-signal bandwidths of the PIN PDs are nearly three times lower compared to those of the VCSELs and thus limit the maximum data rates of the transceivers. First, data transmission experiments were performed in back-to-back (BTB) mode in order to avoid dispersion effects of the glass fiber. As can be seen in Fig. 4, quasi error-free data transmission in half-duplex mode is well possible up to 8 Gbit/s for both word lengths, where about 2 dB more power is needed for the operation with a $2^{15}-1$ long bit sequence. All optical eye diagrams are well open and show little difference between shorter and longer words. A rather limiting case is the free-space operation at 9 Gbit/s for the word length of $2^{15}-1$ bits. Nevertheless, 8 Gbit/s is still the highest data rate ever obtained with bidirectional transceiver chips.

Further investigations into digital data transmission were made using a 500 m long 50 µm core diameter GI MMF with a bandwidth–distance product ($B \times L$) of $\sim 2\,\text{GHz} \times \text{km}$

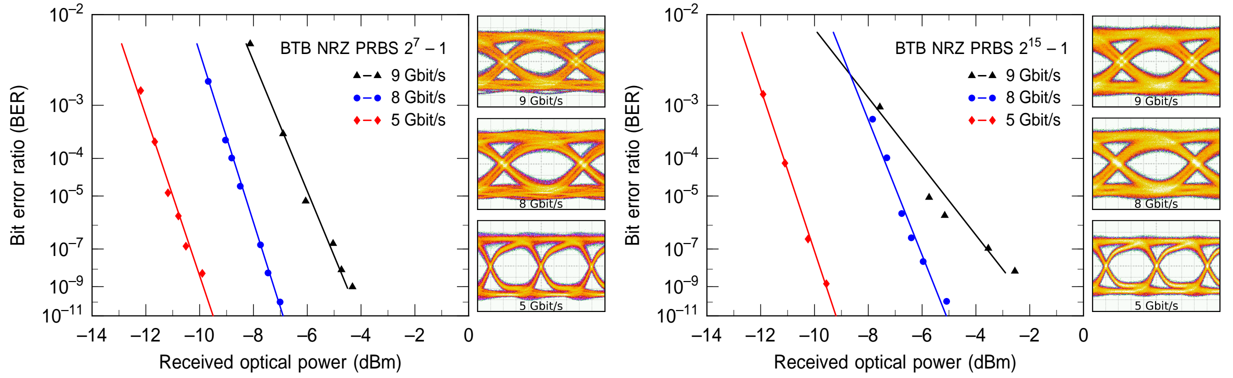

Fig. 4: BER characteristics for BTB half-duplex $2^7 - 1$ (left) and $2^{15} - 1$ (right) word length non-return-to-zero (NRZ) pseudorandom bit sequence (PRBS) data transmission and optical eye diagrams for 9, 8, and 5 Gbit/s.

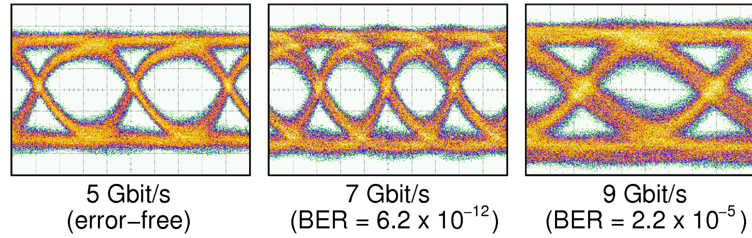

Fig. 5: Optical eye diagrams for half-duplex $2^7 - 1$ word length non-return-to-zero pseudorandom data transmission at 5 Gbit/s (left), 7 Gbit/s (center), and 9 Gbit/s (right), all over 500 m GI MMF.

that was butt-coupled (about 40 µm distance) to each chip. The optical eye diagrams in Fig. 5 indicate quasi error-free data transmission up to 7 Gbit/s. Whereas BTB operation in Fig. 4 (left) was still well possible up to 9 Gbit/s, in this configuration it was limited by the $B \times L$ of the MMF, as can be seen from the higher BER in Fig. 5 (right).

5. Conclusion

In this article, a new kind of monolithically integrated 850 nm wavelength transceiver chip has been presented for bidirectional optical data transmission over standard multimode fibers. The chips consist of PIN photodiodes and oxide-confined, top-emitting VCSELs, integrated to match 50 µm core diameter GI MMFs. The main fabrication steps including the sophisticated selective dry- and wet-etching techniques were introduced.

PIN PDs with a maximum bandwidth of 4 GHz and VCSELs with 11.5 GHz can handle data rates of 9 Gbit/s in back-to-back half-duplex mode. Quasi error-free data transmission over 500 m butt-coupled standard MMF could be demonstrated up to 7 Gbit/s. Full-duplex data transmission experiments and detailed studies of the alignment tolerances will be made in the near future.

References

[1] J.D. Ingham, R.V. Penty, and I.H. White, “Bidirectional multimode-fiber communication links using dual-purpose vertical-cavity devices”, *J. Lightwave Technol.*, vol. 24, no. 3, pp. 1283–1294, 2006.

[2] A.M. Kasten, A.V. Giannopoulos, C. Long, C. Chen, and K.D. Choquette, “Fabrication and characterization of individually addressable vertical-cavity surface-emitting laser arrays and integrated VCSEL/PIN detector arrays”, in *Vertical Cavity Surface Emitting Lasers XI*, K.D. Choquette, J.K. Guenter (Eds.), Proc. SPIE 6484, pp. 64840C-1–6, 2007.

[3] P. Kazlas, J. Wasserbauer, J. Scott, D. Paananen, S. Swirhun, and D. Lewis, “Monolithic vertical-cavity laser/p-i-n photodiode transceiver array for optical interconnects”, *IEEE Photon. Technol. Lett.*, vol. 10, no. 11, pp. 1530–1532, 1998.

[4] M. Stach, F. Rinaldi, M. Chandran, S. Lorch, and R. Michalzik, “Bidirectional optical interconnection at Gb/s data rates with monolithically integrated VCSEL-MSM transceiver chips”, *IEEE Photon. Technol. Lett.*, vol. 18, no. 22, pp. 2386–2388, 2006.

[5] R. Michalzik, A. Kern, M. Stach, F. Rinaldi, and D. Wahl, “True bidirectional optical interconnects over multimode fiber”, in *Optoelectronic Interconnects and Component Integration IX*, A.L. Glebov, R.T. Chen (Eds.), Proc. SPIE 7607, pp. 76070B-1–17, 2010.

[6] S. Salimian and C.B. Cooper, III, “Selective dry etching of GaAs over AlGaAs in $SF_6/SiCl_4$ mixtures”, *J. Vac. Sci. Technol. B*, vol. 6, no. 6, pp. 1641–1644, 1988.

[7] J.-H. Kim, D.H. Lim, and G.M. Yang, “Selective etching of AlGaAs/GaAs structures using the solutions of citric acid/H_2O_2 and de-ionized H_2O/buffered oxide etch”, *J. Vac. Sci. Technol. B*, vol. 16, no. 2, pp. 558–560, 1998.