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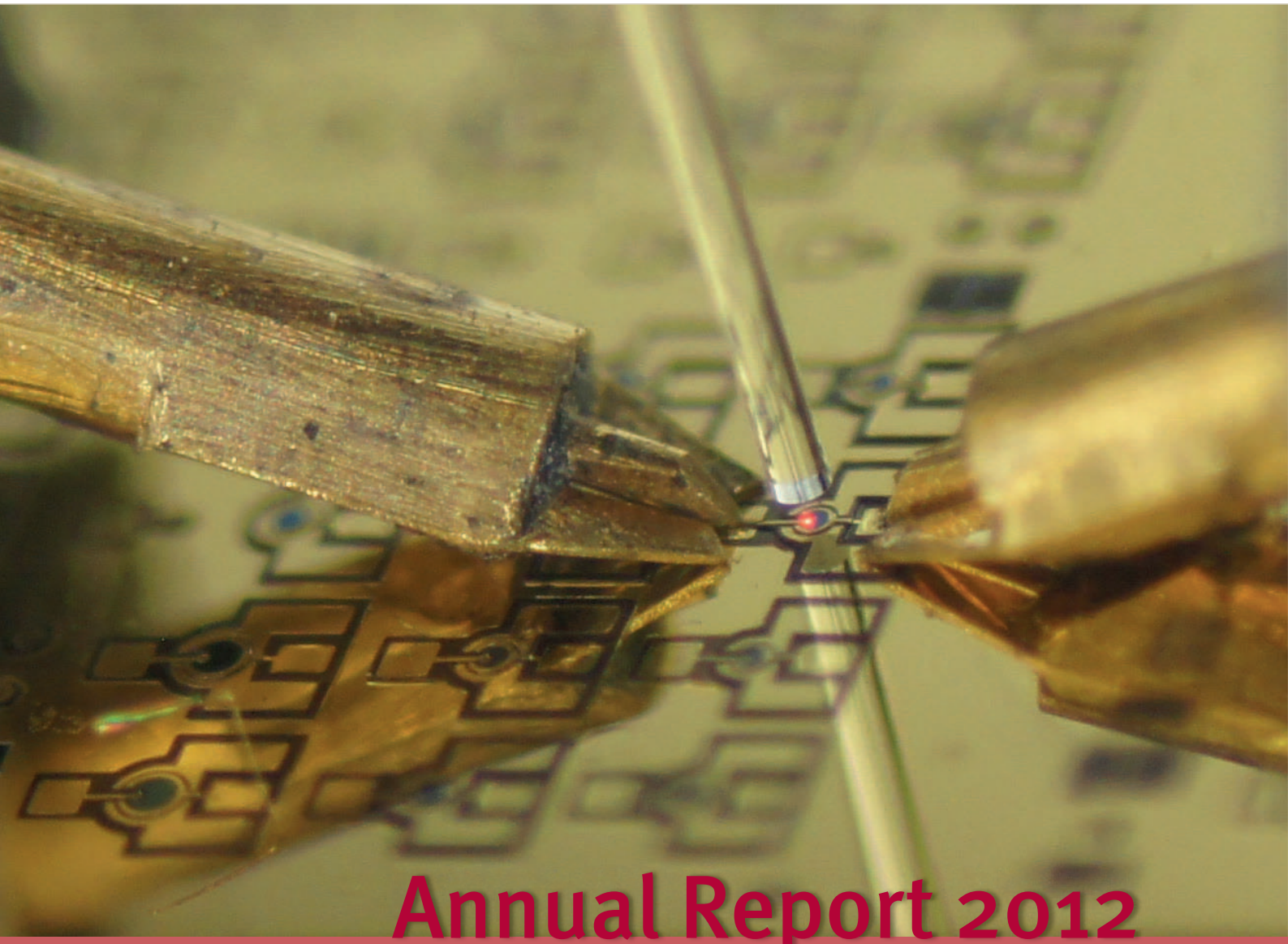

Annual Report 2012

Institute of Optoelectronics

Cover photo:
On-wafer high-frequency testing of an optoelectronic transceiver device for bidirectional data transmission over an optical multimode fiber. A vertical-cavity surface-emitting laser (VCSEL) is monolithically integrated with a PIN-type photodiode. Electrical contacts are established by two ground–signal–ground microwave probes. In the photo, the optical fiber with 125 µm outer diameter is displaced from the chip. For actual operation, the fiber is butt-coupled with a distance of only about 30 µm. See the related article on transceiver chips.

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Preface

In the year 2012, research in the Institute of Optoelectronics progressed a lot. It focused on vertical-cavity surface-emitting lasers (VCSELs), optical interconnect systems, GaN-based electronic and optoelectronic devices, and semiconductor disk lasers.

The VCSELs and Optical Interconnects Group has successfully completed its projects on atomic clock VCSELs and monolithic VCSEL–PIN photodiode chips. Work on optical datacom links and microfluidic-integrated systems is continuing.

The GaN group further concentrated their studies on semipolar GaN epitaxial structures after the approval of the second 3-years phase of our transregional research group PolarCoN at the beginning of last year. Hence, we could arrange another summer school at Kloster Kostenz with more than 40 participants. Moreover, new projects about semipolar yellow LEDs and semi-insulating GaN bulk wafers were launched, while other topics like in-situ electrical measurements on graphene flakes in a transmission electron microscope were successfully continued. We could achieve excellent performance of LEDs grown on quasi-bulk GaN wafers demonstrating the successful synergetic combination of our HVPE and MOVPE studies.

In the High-Power Semiconductor Laser Group, an optically-pumped semiconductor disk laser with an output power of more than 21 W at an emission wavelength of 1040 nm has been realized. Even at a heat-sink temperature of the semiconductor disk of 90 °C, more than 3.5 W of output power has been achieved. In a folded cavity setup including a nonlinear LBO crystal for second-harmonic generation, 9.5 W of green light at an emission wavelength of 520 nm has been obtained. The system shows a conversion efficiency of 20 % with respect to the incident optical pump power and exhibits a tuning range of 22 nm.

The new VCSEL book edited by Rainer Michalzik which was announced in the last Annual Report was eventually published by Springer in early Oct. 2012. Moreover Rainer served as the co-editor of the Special Issue "Recent Advances in Semiconductor Surface-Emitting Lasers" published in *Advances in Optical Technologies*.

Anna Bergmann was selected as a participant of the "Get Ahead With Optics" Summer School for female graduate students of optical technologies from Tunisia and Germany, which was held in Hammamet-Yasmine, Tunisia, in Sept. 2012.

Rainer Michalzik
Ferdinand Scholz
Peter Unger Ulm, March 2013

High-Power Green Laser Sources

Alexander Hein

To access the green spectral range for display applications, high-power optically pumped semiconductor disk lasers (OPSDLs) in combination with second-harmonic generation have been realized. A frequency-doubled output exceeding 9.5 W is achieved at a wavelength of 520 nm. The wavelength of these devices can be tuned over a rather broad range of more than 20 nm in the second-harmonic regime. In this article, operation characteristics and limiting mechanisms of OPSDLs are discussed.

1. Introduction

One of the driving applications for green emitters are display technologies. Gallium nitride (GaN) based direct green laser diodes with continuous-wave (CW) output powers above 100 mW at wavelengths up to 532.1 nm were already reported by Sumitomo Electric and Sony [1]. At lower power levels, wavelengths of up to 536.6 nm have been realized which are closer to the peak of human visual sensitivity at 550 nm. These small-power and low-coherence devices are predestined for pico-projector applications, where high output powers are not needed and easy despeckling is required. However, especially for cinema projection which currently relies on xenon arc lamps, there is an occurring need for high-power laser systems. Well established frequency-doubled solid-state laser systems like Nd:YAG or Nd:YVO_4 are struggling with highly demanding cinema requirements and are difficult to despeckle, whereas a Nd:YLF frequency-doubled system from Laser Light Engines Inc. with optical outputs of 30 and 50 W (Q-switched) meets the requirements since it can be utilized in such a way that the output is despeckled [2]. High-power frequency-doubled OPSDLs are other promising candidates for cinema projection because they draw on the advantages of lower coherence for despeckling and unmatched wavelength tailoring to produce any desired gamut. Additionally, similar to solid-state lasers, the small fiber-coupling losses in these high-beam-quality systems may enable off-board illumination when required.

2. OPSDL Structure and Thermal Management

A more detailed description of the layer structure, design strategy, and preliminary characterization measurements such as photoluminescence and reflectivity spectra for these devices were presented in [3]. The semiconductor layer structure with its key elements is depicted in Fig. 1. To achieve high optical outputs with these devices, proper heat removal is required in order to keep the temperature inside the active region with the quantum wells (QWs) low because of thermal leakage and carrier spill-over for structures

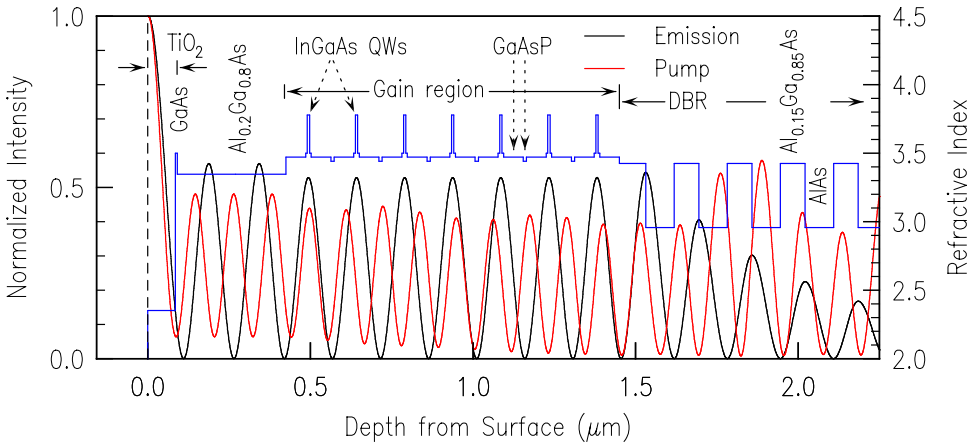

Fig. 1: Refractive index representation of the semiconductor layer structure, complemented by a dielectric anti-reflection TiO_2 surface coating on top. Gain is provided by 7 compressively strained InGaAs QWs surrounded by tensile strained GaAsP pump light absorbing barriers. The structure is finalized by a 56 layer distributed bragg reflector (DBR), transparent for the pump wavelength, and a Ti/Au/Pt/Au metalization. The field intensities of the laser emission and the pump light are also plotted.

with reduced barrier height [4]. Since the heat flux in the semiconductor layers is almost completely one-dimensional it is impossible to extract watt-level heat power from typical pump spot sizes of 500–900 µm. Thus, thick heat spreaders with high thermal conductivities have to be employed. This can be implemented using a transparent intra-cavity heat spreader placed on the semiconductor disk surface to bypass the thermal impedance of DBR mirror and substrate, or as a submount adherent to the mirror where the substrate is removed from a bottom-emitter leaving only a foil of 5–7 µm thickness as the actual semiconductor laser disk. Figure 2 shows secondary electron microscope (SEM) images of a mounted bottom-emitting semiconductor disk on a diamond heat spreader before the substrate was removed.

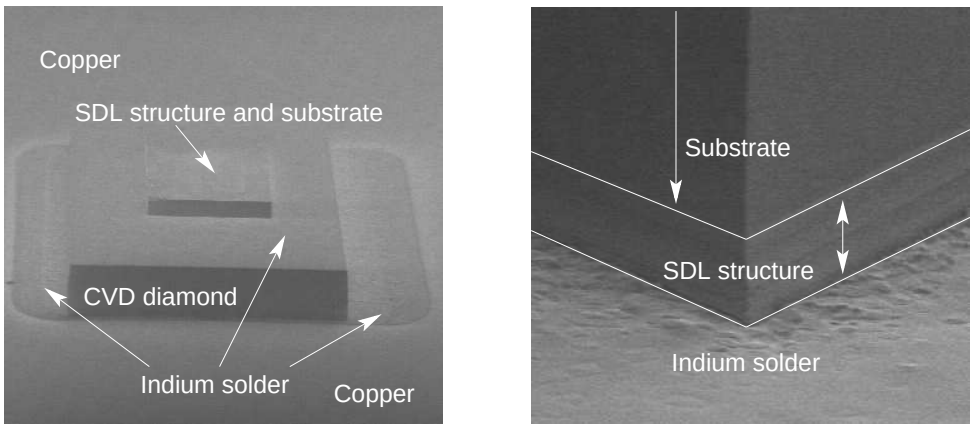

Fig. 2: Semiconductor disk laser with substrate mounted on a CVD diamond heat spreader and a gold-plated copper carrier with a two-step indium evaporation and solder process (left). Enlargement of the disk's edge where the actual device structure can be seen (right).

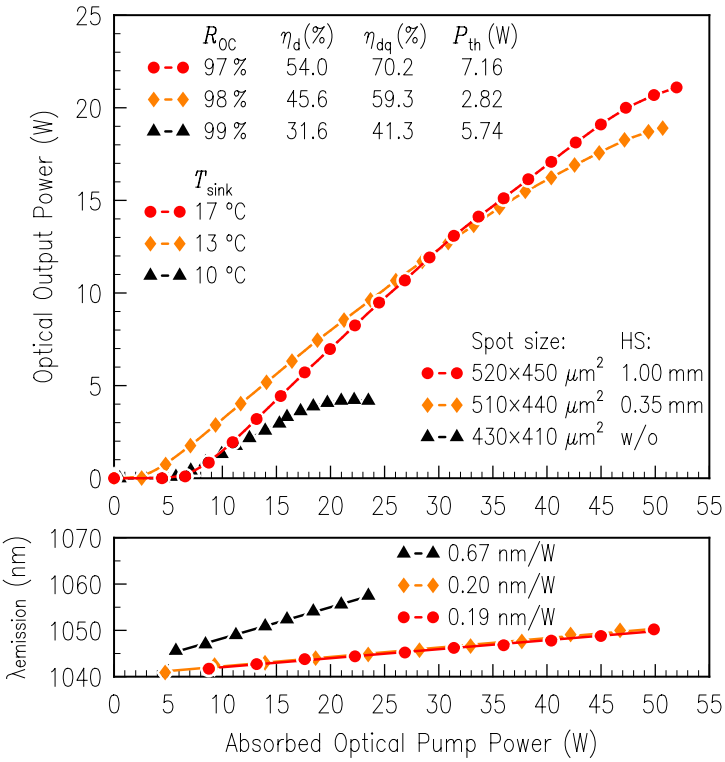

Fig. 3: Comparison of output characteristics for a standard gold-plated copper heat sink device with two devices mounted on CVD diamond heat spreaders with thicknesses of 0.35 and 1.00 mm. The resonator length for all measurements was approximately 140 mm with a mirror radius of curvature of 150 mm, but with output coupler reflectivities R_{OC} chosen for maximum output.

2.1 Heat spreader influence

To efficiently remove the heat from the active region and to increase the output powers of the devices, two different heat spreaders (HS) were investigated. The heat spreader material was chemical vapor deposited (CVD) diamond with thicknesses of 0.35 mm and 1 mm and thermal conductivities of 1800 W/(m · K) and 2000 W/(m · K), respectively. The output characteristics for both devices are depicted in Fig. 3 for a fixed heat-sink temperature. For better comparison and emphasis of the effect, a characteristic of a device without a diamond heat spreader are added in the figure as well. Besides the obvious drastic increase in output power for comparable pump spots and temperatures, the devices with a heat spreader show a much smaller wavelength shift rate per watt of absorbed power. Thermal roll over occurs at an absorbed power of 52 W in case of the thicker heat spreader, while the device with the thinner diamond shows roll-over for a power level of 50 W. The higher output and better slope are attributed to better spreading and heat-transfer characteristics of the thicker heat spreader. However, considering the thickness and accounting for the fact of a 22 % better thermal conductivity, the rather modest increase in output power of 11 % appears to be too small. Since two soldering steps are necessary, fluctuations during these may be an explanation for the only small increase in performance. However, since the point of thermal roll-over is very similar,

the explanation is unsatisfactory and the limit is rather set by the cooling circuit of the system. When the cooling capacity is high enough, output powers in excess of 100 W can be generated by the excitation of larger areas and the use of thicker heat spreaders [5].

2.2 Temperature influence

As reported in [6], changes in the power characteristics with temperature can be used to extract some properties of the OPSDLs. Optical output powers at different heat-sink temperatures are depicted in Fig. 4. The heat-sink temperature was increased from 20 °C to 90 °C in steps of 10 °C, while the output power was recorded until the rollover point. Any other parameters such as cavity length, pump spot size, etc., were kept constant. The maximum extracted output power at 20 °C was 21.5 W and gradually dropped to 3.5 W for a heat-sink temperature of 90 °C. Measurements at higher operation temperature were not performed since the thermoelectric Peltier cooler used for temperature stabilization had a maximum specification of 100 °C. Taking the dissipated heat power, which is given by the relation

$$P_{\mathrm{diss}} = P_{\mathrm{abs}} - P_{\mathrm{out}}, \tag{1}$$

where P_{abs} is the absorbed power and P_{out} is the optical output power, as a function of the respective heat-sink temperature, essential temperature characteristics can be derived as indicated in the left part of Fig. 5. By applying a linear fit to the data points at rollover, the internal shut-off temperature can be extracted from the intersection with the abscissa. For levels above 50 W of absorbed pump power, heat-sink temperatures of 20 °C and 30 °C could not be maintained, so the linear fit only accounts for heat-sink temperatures above 30 °C. For our devices, the roll-over temperature is determined to 145 °C. From the slope it is evident, that, in order to dissipate an additional watt of heat at rollover, approximately a 3 °C lower heat-sink temperature is required. Accounting for a quadratic increase of the threshold pump power, which is included in the dissipated heat term, and for a linear drop in slope efficiency with increasing heat-sink temperature as indicated in the right part of Fig. 5, watt-level operation should be possible at even 110 °C. At 120 °C, the required threshold power is already higher than the maximum possible

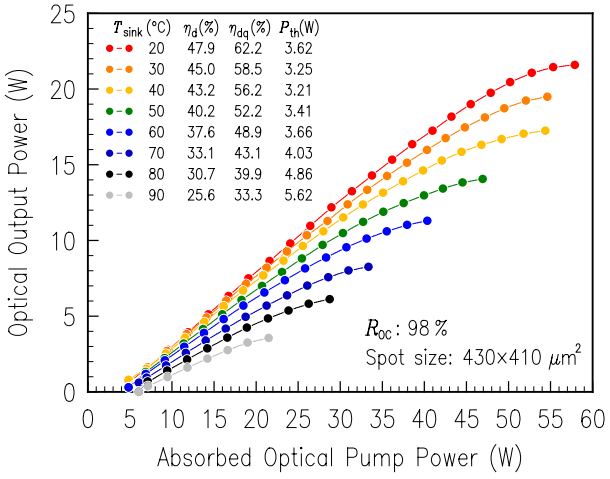

Fig. 4: Output power characteristics for a device with a 1 mm-thick diamond heat spreader up to thermal rollover for heat-sink temperatures T_{sink} from 20 °C to 90 °C. The behavior of slope efficiency η_{d}, differential quantum efficiency η_{dq}, and threshold pump power P_{th} are listed in the legend.

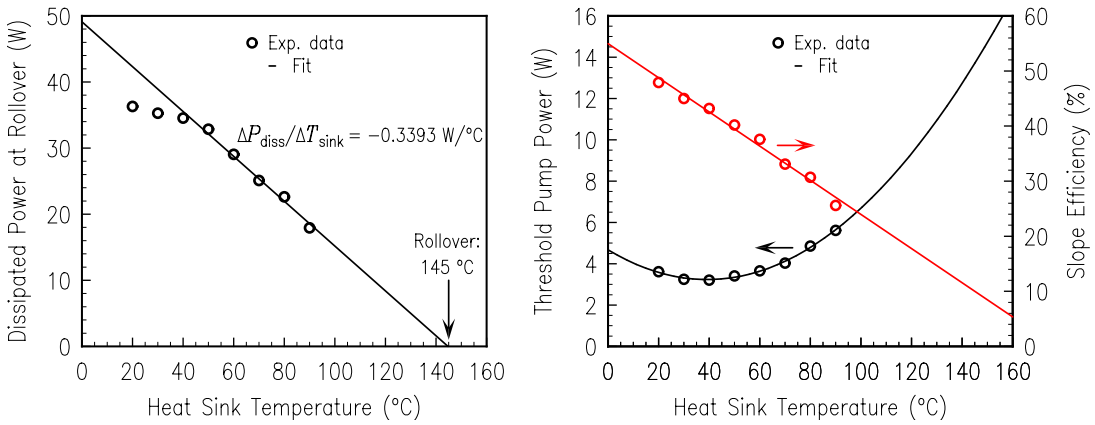

Fig. 5: Dissipated heat power at thermal rollover in dependence of the heat-sink temperature (left). Threshold pump power and slope efficiency vs. heat-sink temperature (right).

heat dissipation at roll-over, so the absolute maximum operating temperature should be around 116–119 °C. It should be noted that the sensor used is specified with an accuracy of ±1 °C. Considering the deviations of the dissipated power at rollover from the linear regression for heat-sink temperatures of 20 °C and 30 °C, it is plausible that the cooling capacity was insufficient and underlines the described heat-sink temperature increase at high pump levels. Proper backside heat dissipation of the thermoelectric cooler or larger dimensioning should lead to higher dissipated heat levels and subsequently higher optical outputs.

3. Green Output

Compared to the results reported in [7], the cavity was modified in order to yield one main output of the second-harmonic (SH) emission through the folding mirror as indicated in Fig. 6, with specified reflectivities for the fundamental and second-harmonic of 99.99 % and < 2 %, respectively. The minor frequency-doubled output from the end mirror was used to monitor and record the emitted wavelength. Polarization and wavelength were controlled via a 4 mm thick birefringent filter (BRF) located in the longer cavity arm. Results obtained with the cavity configuration as pictured in Fig. 6 are summarized in Fig. 7. The second-harmonic output for all three wavelengths was mainly limited by an increase of the heat-sink temperature at pump power levels of 45 W and above. The two curves for the shorter wavelengths yield clearly better output and efficiency characteristics. However, the increasing internal temperature gradually favors the emission at the longer wavelength which explains why at maximum output the curve shows no behavior of a decreasing slope compared to the shorter wavelengths. This is also seen in the steadily rising conversion efficiency of that particular curve. Throughout all measurements, the output was extremely stable, attributed to temperature stabilization of the nonlinear crystal, which was not yet applied in [3]. It was observed that the crystal temperature is steadily rising as long as the input power is increased, thus, changing the phase matching conditions [8]. Adaptation of the crystal angle is then necessary to regain a phase-matched condition.

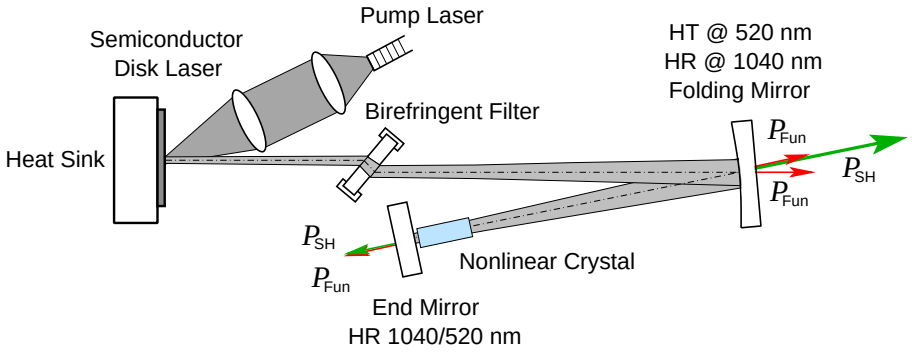

Fig. 6: Folded resonator configuration with highly reflective single (HR/HT) - and double-band (HR/HR) external mirrors enabling a main high-power output of the frequency-converted radiation.

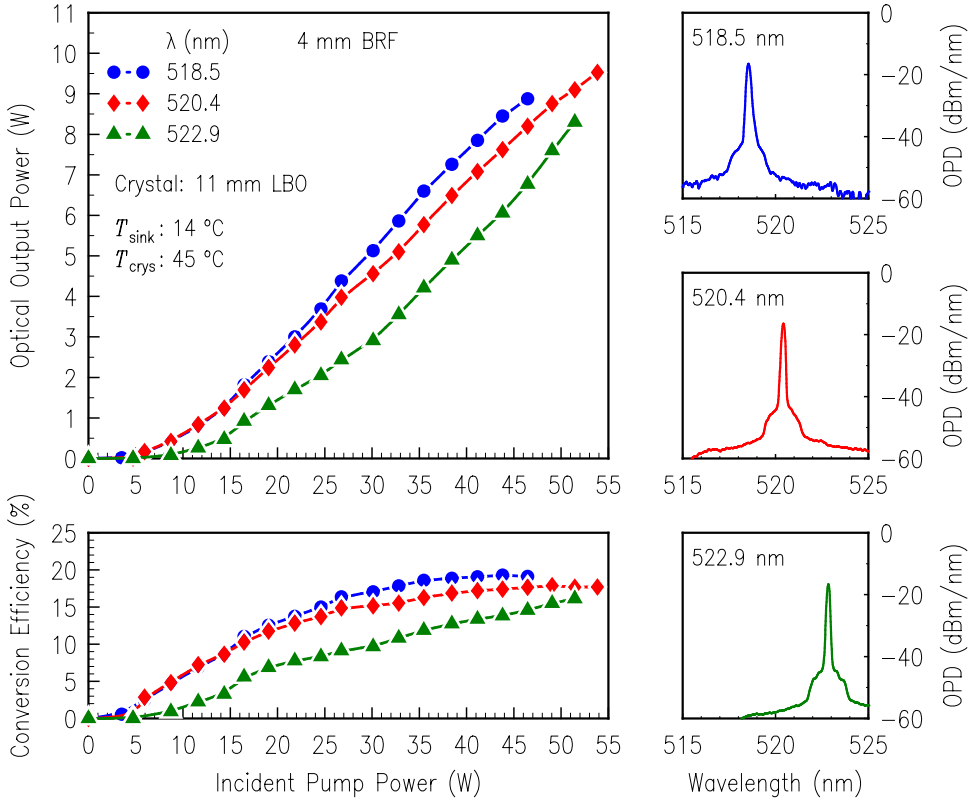

Fig. 7: Second-harmonic output powers and conversion efficiencies for different emission wavelengths. The output powers were generated at a heat-sink temperature of 14 °C, while the temperature of the 11 mm lithium triborate (LBO) crystal was stabilized at 45 °C. Tuning to the respective wavelengths was achieved by rotation of the birefringent filter.

Further improvements to achieve higher efficiencies would require to suppress the rather high losses with a perpendicular polarization caused by the birefringent filter as observed in [9]. Since SDLs are inherently broad gain devices they are also capable of a rather broad tuning range in the SH regime. In operation, the wavelength was shifted by rotating a 2 mm thick BRF around its optical axis without any other adjustments to the cavity

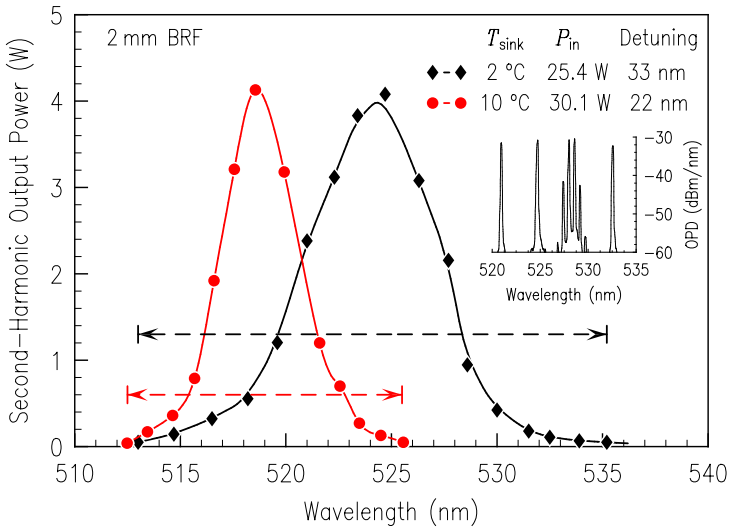

Fig. 8: Output power vs. wavelength in the second-harmonic regime for two devices with different detuning of micro-cavity resonance and QW peak wavelength, and different heat-sink temperatures. The inset shows various recorded spectra during the tuning experiment for the device with the broader tuning range.

or the angular position of the crystal. The measurement was performed on two devices with different detuning (micro-cavity resonance vs. QW peak wavelength) characteristics, as shown in Fig. 8. The obtained tuning bandwidth was 22 nm, ranging from 513 nm to 535 nm for a device with a determined detuning of 20 nm at room temperature. At these boundary values an optical output of roughly 60 mW was measured. A maximum power of 4.1 W was obtained at 524.7 nm. The full-width-at-half-maximum (FWHM) bandwidth with 2 W of SH power is 7 nm. For the second device it is a 13 nm bandwidth for a similarly high optical output at the optimum wavelength. Devices with a smaller detuning naturally yield a narrower tuning range. For certain wavelengths there were multiple peaks indicating parasitic etalon effects, as provided in the inset of the figure, but these could be eliminated by smaller adjustments to the cavity. The origin of these parasitics is not fully understood. The shortest possible wavelength around 513 nm for both devices originates from the fact of a wafer-position-independent QW peak wavelength and the support of the lower heat-sink temperature for the device with the larger detuning. The longest wavelength is simply governed by the micro-cavity resonance, which is red-shifted by 12 nm for the large detuning device.

4. Conclusion

In this work, efficient high-power frequency-doubled semiconductor disk lasers have been realized. High-power operation in the fundamental regime of more than 20 W was achieved with an elaborately designed semiconductor structure and the implementation of a CVD diamond heat spreader. High-temperature operation of the devices up to 110 °C seems possible regarding the extrapolation of the experimental results. In the second-harmonic regime an output power close to 10 W (9.5 W) has been achieved at 520 nm. The tuning

range of the devices under test is as wide as 22 nm for the green output, depending on the detuning properties and operating temperatures.

Acknowledgment

The assistance of Susanne Menzel and Rudolf Rösch with growth and device processing as well as of Andreas Ziegler and Markus Rampp with various measurements is gratefully acknowledged.

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VCSELs With X-Shaped Cavity: Cool and Fast

Hendrik Roscher and Rainer Michalzik

We present a novel type of AlGaAs/GaAs-based vertical-cavity surface-emitting laser (VCSEL) and two-dimensional arrays with an X-shaped cavity cross-section which we term XCSEL. The devices are cool in the sense that they have record-low thermal resistances after flip-chip bonding and substrate removal, which will allow high-density hybrid integration with electronic circuitry in future optical interconnects. Common approaches for efficient heat removal increase the parasitic laser capacitance and limit the operation speed. This effect is minimized in the new devices — they also remain fast.

1. Introduction

VCSELs are firmly established coherent light sources in optical sensing and data communications [1]. The overwhelming majority of commercial devices is based on GaAs quantum well (QW) technology for emission wavelengths in the 840–860 nm spectral window. This holds for both position sensors like optical computer mice and optical interconnects over multimode fiber (MMF). The latter topical area has gained much momentum in recent years. All major VCSEL companies are intensively working on next-generation higher-speed devices to keep up with the growth predicted in roadmaps of, e.g., the InfiniBand or Fibre Channel standards. Data rates of 25 to 28 Gbit/s data rates are the next step for commercial VCSELs.

In order to be a viable alternative to electrical lines, a higher channel count of optical intra-system links is needed over shorter and shorter distances [2]. Simultaneously there is a strong need for cost reduction. Moreover, compared to established data communications transceivers, a transmitter formed by the hybrid integration of VCSELs with electronic circuits will experience higher ambient temperatures which are known to reduce laser reliability in an exponential way [3]. Hence, for such systems, high-speed VCSEL arrays are sought which can be manufactured at lower cost, can be integrated with electronics, and show reduced self-heating. We attempt to take a step in this direction by proposing a novel type of 850 nm VCSEL and two-dimensional (2-D) array that provide such benefits without obvious drawbacks for their dynamic performance.

We will briefly introduce the novel device concept and the fabrication approach. Thermal properties of manufactured prototype lasers as well as their static and dynamic characteristics are then presented.

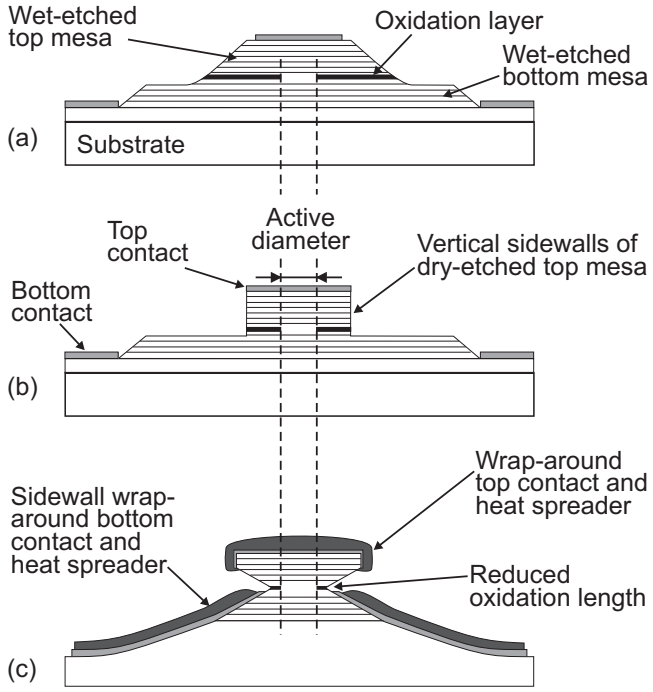

Fig. 1: (a) Conventional wet-etched VCSELs. (b) Conventional dry-etched VCSELs with vertical top mesa sidewalls. (c) XCSEL exhibiting the characteristic X-shaped outline.

2. Device Concept

The basic idea behind the new scheme is both simple and effective: instead of eliminating the influence of the sidewalls, they are utilized in a new way with benefits for both the fabrication as well as the performance of the lasers. It is not attempted to alleviate surface topography to apply planar technology but useful three-dimensional profiles are shaped in the wafer surface. This involves a novel shape forming of VCSEL sidewalls using a generic etch process by simply exploiting etch rate differentials between layers of different material compositions. In a simple case, this may produce vertical sidewalls with one circumferential geometric constriction as in an hourglass.

Part (c) of Fig. 1 shows an exemplary schematic cross-section of such a device in comparison to conventional wet-etched (part (a), see also [4]) and dry-etched (part (b), see also [5]) VCSELs. In conventional wet-etched VCSELs, tolerances for manual contact lithography impede further miniaturization. Large and poorly defined oxide widths lead to deviations of active diameters, parasitic capacitance, and blockages to heat flow. There is moreover no possibility to integrate efficient cooling structures. The vertical mesa sidewalls in part (b) are obtained by relatively expensive dry-etching techniques that somewhat reduce the oxide width and ensure a better reproducibility of the active diameters. The new device in part (c) has both optimized properties and requires substantially fewer processing steps. The notch in the center has consequences for the 1) guiding of the optical field in the laser, 2) current injection, 3) heat extraction from the core of the device, and 4) overall strategy of fabrication. By giving the sidewalls a structure that includes notches or constrictions with sections of negative sidewall angle, it becomes possible for the first time to truly control a structured metal deposition in the vertical dimension with sub-micrometer precision. As a consequence, integrated cooling structures compatible with high-frequency modulation are possible.

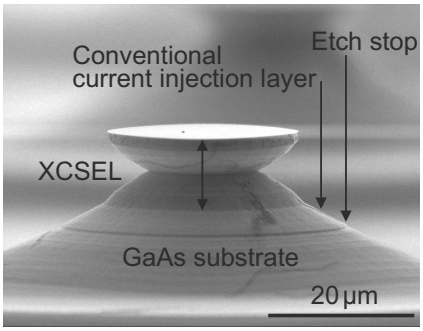

Fig. 2: SEM image of a typical XCSEL with a small sidewall constriction.

Figure 2 shows a scanning electron microscope (SEM) image of an example fabricated XCSEL. There is a conventional lateral current injection layer of around 3 µm thickness visible in the image which is actually not needed. Typical values for the lateral etch depth under the edge of the resist mask are 20 µm and 30 µm. The former produces a smaller sidewall notch and leaves a portion of the top mirror with more or less vertical sidewall as in Fig. 2, while the latter value produces notches spanning the entire top mirror. A mask was designed for arrays with 4×8 elements and 8 different VCSEL sizes with diameter increments of 2 µm.

3. Self-Aligned Hybridized XCSEL Arrays

An overview of a complete substrate-side-emitting flip-chip XCSEL structure is displayed in Fig. 3. Remarkably, despite of its complex shape, this structure takes much less effort to make than previous versions of flip-chip VCSELs. In the final state shown in Fig. 3, all of the substrate is removed, reducing the XCSEL to only the cavity and mirror layers. Prior to the injection of an underfill, the structure is free-standing, however stable enough for normal laboratory handling while measurements are performed. In order to demonstrate how far the XCSEL approach can be taken, the devices were fabricated with integrated mechanical guides to aid the alignment of optics. There is also an efficient through-connection for the bottom contact.

A main characteristic of XCSELs is the strongly improved thermal management. While all direct-mesa solder-bonded VCSELs have a good thermal connection of the mesa top to the solder joint, in XCSELs the top distributed Bragg reflector (DBR) sidewalls are also wrapped with metal without any passivating, and hence heat-blocking, interlayers. However, the biggest gains in heat flux in XCSELs versus conventional VCSELs are expected by the heat spreaders leading from the central cavity over the sidewalls of the bottom DBR to the optically contacted side of the lasers. These heat spreaders immediately access the inner heat source and transport heat away from there toward the optical side of the chip stack. This is the side that lends itself to cooling, since passive optics do not emit any additional heat.

In XCSELs, initially created profiles in the wafer surface are the basis for all subsequent processes. These profiles are the result of two lithography and subsequent wet-etching steps. Along with the actual laser profiles, spikes are created that lack any overhangs in their sidewalls. Once the profile is created and metal covered for electrical and thermal

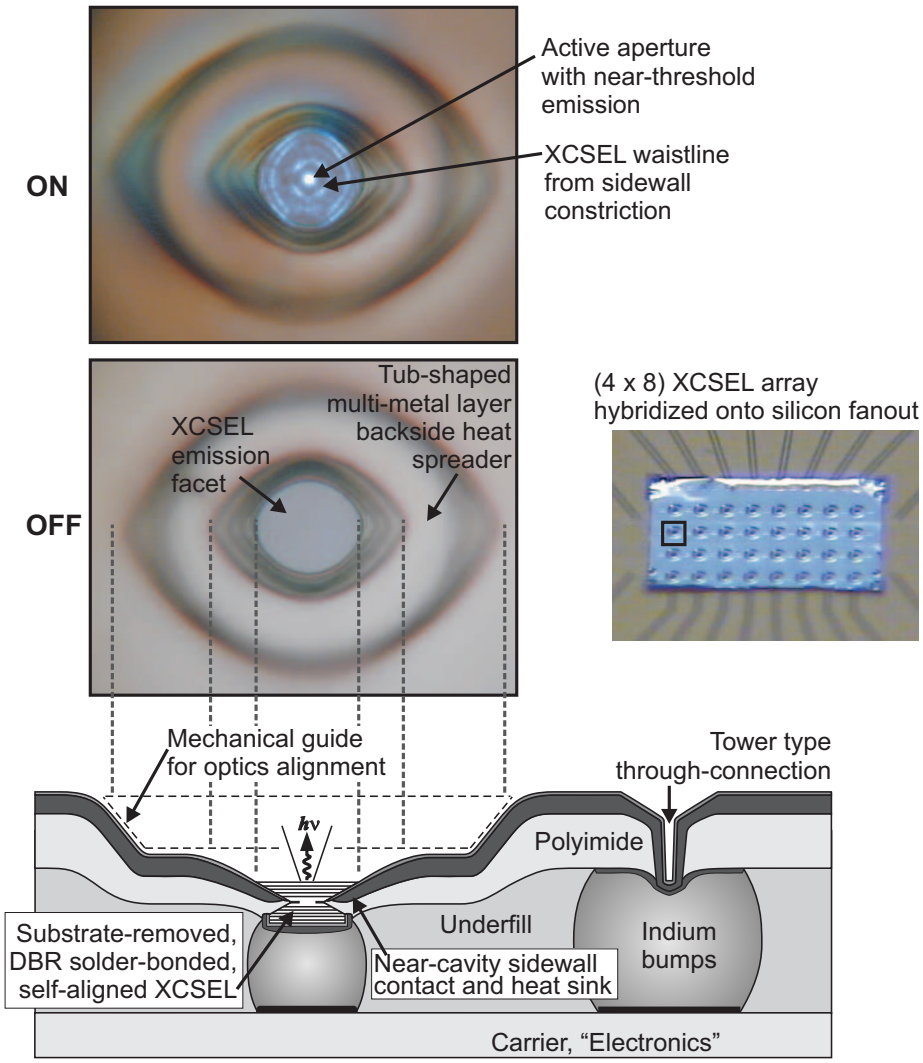

Fig. 3: Overview of the fabricated structure: fully self-aligned direct-mesa solder reflow flip-chip bonded 4×8 XCSEL array, each laser including an optics alignment guide. The schematic at the bottom gives a cross-section of one cell in the hybridized laser array that is shown after placement onto a silicon carrier with address lines in the right-hand photograph. The left-hand photographs are close-up views of the emission side of one XCSEL in this array, both in off and on state.

conduction, the procedure that provides the flip-chip interfaces is simple: the entire surface structure is cast in a single layer of a suitable polymer. After the polymer is hard-baked, it is plasma-etched to simultaneously expose the XCSEL top DBR and the top of the through-connection towers.

Conventional processing methods are employed to implement the flip-chip interface. The left-hand image of Fig. 4 shows the plated solder pads wrapped around the XCSELs and through-connections while still embedded in the plating resist. The two images to the right show the pads after resist removal. The plating base is still present in these images. Eventually the solder is deposited in the same way as was explained in [5] to provide flip-chip-ready lasers.

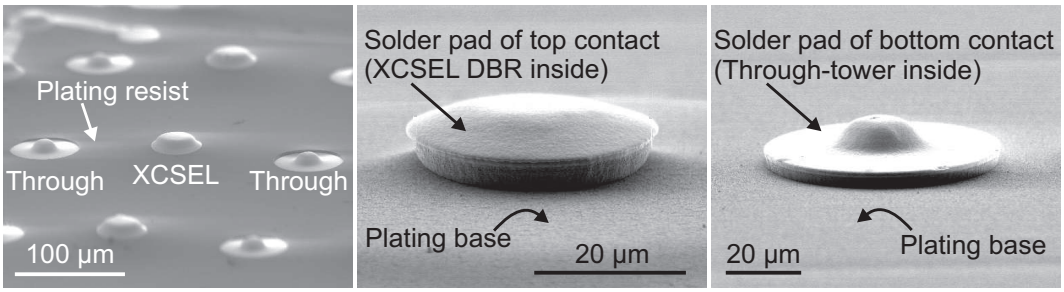

Fig. 4: SEM images of about 5 µm thick plated solder pads wrapped around the top parts of the XCSELs and through-connections. In the left-hand image the pads are still embedded in the plating resist while in the two images to the right the resist has been removed.

4. Experimental Results

4.1 Thermal properties

Appropriate heat management is a key to VCSEL performance, for which the thermal resistance is a convenient global measure. It is defined as $R_{\mathrm{Th}} = \Delta T / P_{\mathrm{diss}}$, where ΔT is the average temperature increase and P_{diss} is the dissipated power in the device. Except for thermal tuning schemes, a low thermal resistance is normally desired to limit self-heating. This permits efficient high-current operation throughout the operating life. In high-speed applications, excessive junction temperatures cause the resonance frequency to saturate. In many instances such as the direct flip-chip integration of VCSELs to electronic circuitry, the lasers are attached to hot surfaces and cannot rely on active cooling through a heat sink. That is, they are densely integrated with other heat sources rather than with heat sinks. When many heat sources are densely packed, the overall package has to ensure efficient heat flow.

Figure 5 provides an overview of thermal resistances for a large range of devices. Extensive data from previous works is included for comparison (sorted by year): Lear1995 [6], Mathine1996 [7], Wipiejewski1996 [8], MacDougal1998 [9], Pu1999 [10], Krishnamoorthy2000 [11], Teitelbaum2004 [12], Al-Omari2005 [13], Al-Omari2006 [14], Demir2011 [15]. U-L-M2007 is a typical value for commercial oxide-confined on-substrate devices. Very low thermal resistance values were reported more than a decade ago [8] for on-wafer-measured air-post devices, where the active diameter is defined by the diameter of the pillar etched into the top DBR. These devices retained their substrate through which the backside contact is provided. They are apparently not fully isolated, since the bottom DBR as well as the active region layers were left untouched. This structure was buried under 15 µm of plated Au spanning an area of $300 \times 300\,\mu\mathrm{m}^2$ for heat spreading, and thereby creating a large interface with the opposite polarity DBR, which precludes high-speed modulation for data transmission.

High-speed devices with conventional sidewall heat spreaders were more recently fabricated with the objective of lowering the thermal resistance by sidewall heat extraction. The oxide-confined devices in [13] are 850 nm top-emitting on p-substrate and have a copper heat sink on 200 nm of SiN_x wrapped around dry-etched mesas. In [14], a similar

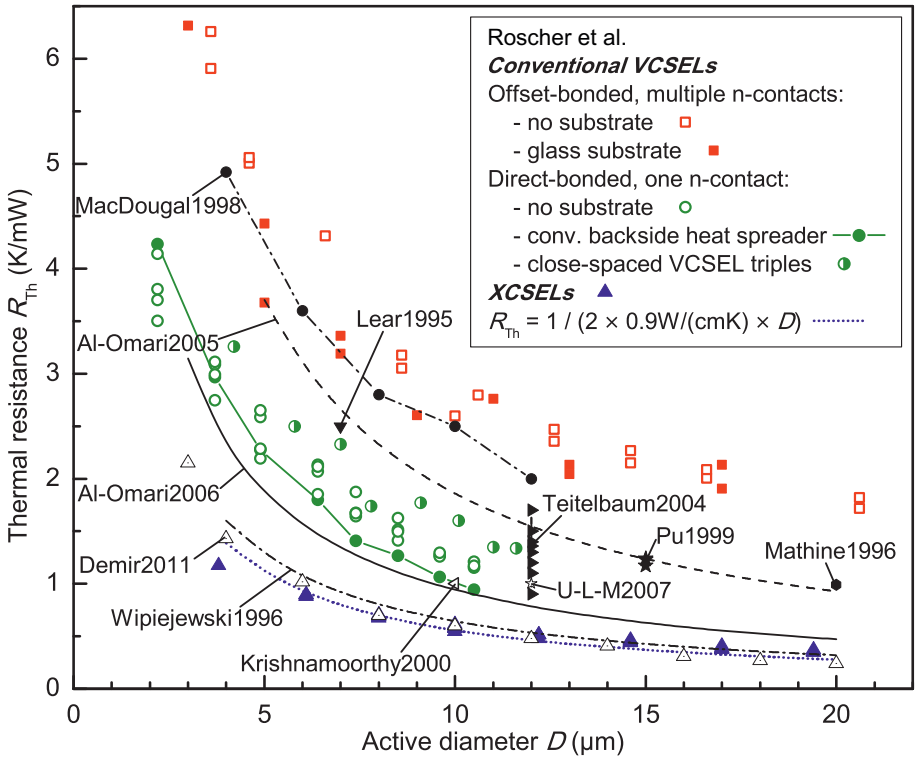

Fig. 5: Overview of thermal resistances achieved for many device configurations. For comparison, data from previous works is included, indicating the first author and year of publication for convenient reference. Corresponding publications are provided in the text.

configuration is used for 980 nm top-emitting VCSELs on n-type substrate. The lasers directly measured on-wafer showed bandwidths up to 16 and 10 GHz, respectively.

Not many details about the "lithographic VCSEL" structure (Demir2011 data in Fig. 5) are revealed in [15], except that these devices are oxide-free. The thermal resistance values were measured on-wafer with thermal power dissipation through the native substrate. These devices are not implemented in a hybridized array configuration. Their modulation properties are not demonstrated.

Even with the early fabricated XCSELs, the thermal resistances were cut by half with respect to previous direct-mesa-bonded VCSELs (see the circles in Fig. 5). These are the best values achieved to date and they even compare favorably with the values of devices from [8] that are aggressively designed for low thermal resistance, have a much less complex structure, and are not capable of any high-frequency modulation. Since then, VCSEL technology has seen the introduction of oxide apertures, hybridization techniques including flip-chip bonding and substrate removal, all of which are used for high-speed applications. XCSELs incorporate this, cut down on processing effort, and bring the thermal resistance to extremely low values, for instance to 0.55 K/mW for a 10 µm active diameter device. The full upright triangles in Fig. 5 show 26 XCSELs indicating good consistency.

In order to obtain the simple analytical expression [16] $R_{\mathrm{Th}} \approx 1/(2\lambda_{\mathrm{c}} D)$ for the thermal resistance in Fig. 5, the VCSEL structure is assumed to be a small disk with diameter D

from which heat flows into a half-space filled with material of thermal conductivity λ_c, where D is taken to be the active device diameter and λ_c is mainly determined by the substrate or heat sink materials. According to the dotted curve described by this equation (see the inset of Fig. 5), this frequently applied law still describes the behavior quite well, given the fact that the actual configuration has little resemblance with the underlying model. It seems, however, to overestimate the increase in R_{Th} as the devices shrink in size and active diameters. Apparently, heat extraction through the circumference of the active region by sidewall heat spreaders becomes more important as the diameters shrink. This is even more true for these devices, since they had a large spread of oxidation lengths, with 4.5 µm for the largest and 5.5 µm for the smallest XCSELs, an about 30 % increase due to the stronger curvature of the oxidation front. A better fit of the data would be achieved if an exponent were included in the denominator of the equation. However, this is avoided since with its present form, an effective material conductivity, with which the imaginary half-space should be filled to achieve the same heat flow from a point heat source, can be derived. With 0.9 W/(cm K), this effective conductivity is about twice as large as that of GaAs (0.45 W/(cm K)), which demonstrates the effectiveness of heat transport in XCSELs.

4.2 Static and dynamic performance

An exemplary XCSEL with 7 µm active diameter has a threshold current of 1.6 mA. After normal processing, ending with substrate and etch-stop removal, the device has a differential resistance of approximately 110 Ω in the current range between 5 and 15 mA. The differential quantum efficiency is 65 % and roll-over occurs at 17.1 mA with 10.1 mW maximum output power. The emission spectrum is similar to that of conventional multimode VCSELs. The far-field profile shows a typical donut-like shape that is a consequence of current crowding and spatial hole burning, leading to preferential pumping of higher-order modes.

Beside having produced the best thermal performance so far demonstrated for this device configuration, XCSELs show attractive dynamic properties. For testing the dynamic performance of flip-chip bonded XCSELs, a carrier is required with transmission lines to address each device. The effects of these lines are contained in the results, since no means were readily available to characterize them separately for de-embedding purposes. An early design of a 4×8 carrier was employed for all XCSEL measurements, whose transmission lines were intended for much lower frequencies than are achievable with today's devices. Moreover, this carrier has large bond pads with 60 µm diameter. For the reflow flip-chip soldering to work properly, evenly large bond pads had to be placed over the XCSELs and an appropriate amount of indium solder deposited. These large pads introduce capacitance, while they are not responsible for the good thermal performance since the solder joint cross-section has not been identified as major bottleneck for heat transport.

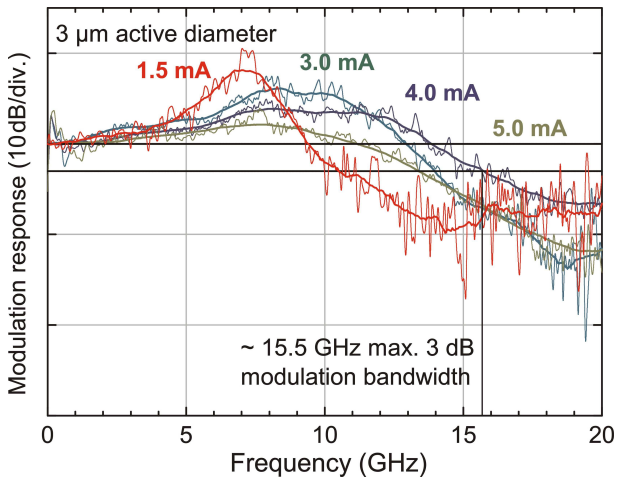

Fig. 6: Small-signal modulation transfer functions of an XCSEL on an early silicon carrier for different operating currents above threshold.

Figure 6 shows the measured small-signal modulation transfer functions for different currents I. Adjacent averaging has been applied to the as-measured curves (thinner lines) to obtain the smoothed curves (thicker lines) that help to determine the corner frequencies. The XCSEL has an active diameter of 3 µm, a large oxidation length of 13 µm, and large 60 µm diameter bond pads. A maximum 3-dB modulation bandwidth of around 15.5 GHz is achieved at 4 mA drive current. From the curves one can extract the corner frequencies $\nu_{3\,\mathrm{dB}}$ as a function of $\sqrt{I - I_{\mathrm{th}}}$, and with a threshold current $I_{\mathrm{th}} = 1\,\mathrm{mA}$ obtain a modulation current efficiency factor $\mathrm{MCEF} = \nu_{3\,\mathrm{dB}}/\sqrt{I - I_{\mathrm{th}}}$ of approximately $8\,\mathrm{GHz}/\sqrt{\mathrm{mA}}$.

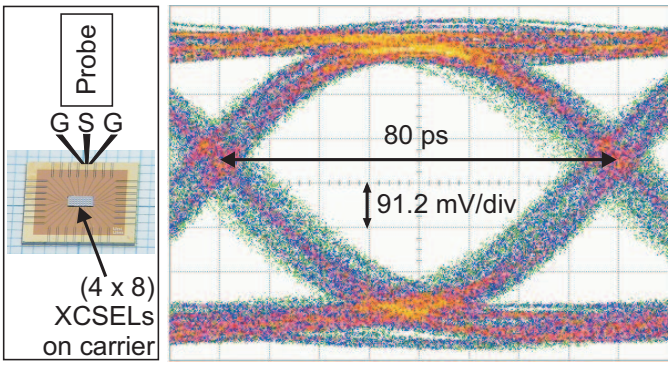

Fig. 7: Photograph of the XCSEL array on a carrier fanout chip with a schematic contact arrangement of a microwave probe (left) and 12.5 Gbit/s eye diagram for modulation with a $2^7 - 1$ word length pseudorandom bit sequence (right).

For testing under digital modulation, only a 12.5 Gbit/s bit pattern generator was available. Figure 7 depicts an optical eye diagram recorded at this data rate. The XCSEL was operated at 3.5 mA bias current and modulated with a peak-to-peak voltage of 1.5 V. While the slow rise and fall times are attributed to the limited receiver bandwidth (an 8 GHz photoreceiver and a 10 GHz amplifier were employed), the eye diagram demonstrates that these devices are suitable for digital data transmission applications at these bit rates. The left part of Fig. 7 shows the entire XCSEL array and the flip-chip carrier described above.

5. Conclusion

We have introduced a novel fabrication approach to flip-chip-bondable 850 nm VCSELs and one- or two-dimensional VCSEL arrays. A unique sequence of wet-etching steps allows us to deposit contact metals close to the region of major heat generation, which reduces the thermal resistance to much improved levels compared to conventional substrate-less VCSELs. Simultaneously the etching sequence readily establishes a flip-chip interface and a surface topology which might prove useful for direct butt coupling to arrays of optical fibers. Fully functional arrays of such XCSELs have been fabricated and equipment-limited digital modulation at 12.5 Gbit/s was demonstrated.

It is worth to point out that the epitaxial layer sequence used for XCSEL production has not been optimized for high-frequency operation. We believe the increase in modulation bandwidth we have seen in XCSELs compared to conventional VCSELs (that were fabricated with similar epitaxial material) is a result of better thermal management that does not interfere with high-frequency circuit properties. The present data were obtained with largely non-ideal devices. Immediate improvements are evident with minimized oxide widths, adjusted bond pad sizes, and shorter address lines on the carrier. Moreover, with common techniques like quantum well strain engineering or photon lifetime adjustment, we can expect that there is much room for improvements of the laser dynamics.

Acknowledgment

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Optoelectronic Bidirectional Transceiver Chips: Crosstalk and Alignment Issues

Alexander Kern

We present the static operation properties of monolithically integrated 850 nm wavelength AlGaAs/GaAs-based vertical-cavity surface-emitting lasers (VCSELs) and PIN (p-doped–intrinsic–n-doped) photodiodes (PDs). Devices with three different epitaxial layer structures of the PDs are investigated. PDs with a 3 µm thick intrinsic region show a responsivity of $> 0.6\,A/W$ and have the lowest dark currents. We investigate the mutual influence between the closely integrated optoelectronic devices. The optical crosstalk is below -11 dB and the maximum electrical crosstalk between VCSEL and PIN PD of around -50 dB is nearly negligible. Butt-coupling to a multimode fiber with a core diameter of 50 µm has maximum fiber alignment tolerances in the range of 14–26 µm.

1. Introduction

For some years we have been doing research into novel transceiver (TRx) devices which integrate VCSELs and PIN PDs for operation in the standard wavelength regime at around 850 nm wavelength. The stacked layer structure requires sophisticated fabrication methods but enables the use in bidirectional short-reach optical data links over a single butt-coupled standard multimode fiber (MMF). Chip fabrication is described in [1] in some detail. As can be seen in Fig. 1, all transceiver device contacts with ground–signal–ground configuration are accessible from the top by two coplanar microwave probes for PD and VCSEL. Thus, static and high-speed operation of the devices is enabled on-wafer without the need for chip separation.

Recently we have reported error-free (bit error ratio $< 10^{-12}$) data transmission experiments (1) at 7 Gbit/s (half-duplex) and 6 Gbit/s (full-duplex) over 500 m of an OM3-type MMF [2], (2) at 8 Gbit/s (full-duplex) in back-to-back operation [1], and (3) at 11 Gbit/s (half-duplex) and 10 Gbit/s (full-duplex) over 550 m OM4 MMF and even at 12.5 Gbit/s (full-duplex) back-to-back [3]. In this report we focus on the static operation characteristics of latest-generation TRx chips and investigate electrical and optical crosstalk as well as the alignment tolerances for butt-coupling to a 50 µm core diameter MMF.

2. Static Device Characteristics

2.1 Transceiver VCSEL

The miniaturized integrated VCSEL with a mesa diameter of 25 µm has an oxide-confined current aperture of 6.4 µm for multimode operation. Figure 2 shows the output characteristics of such a top-emitting device for four different ambient temperatures. The threshold

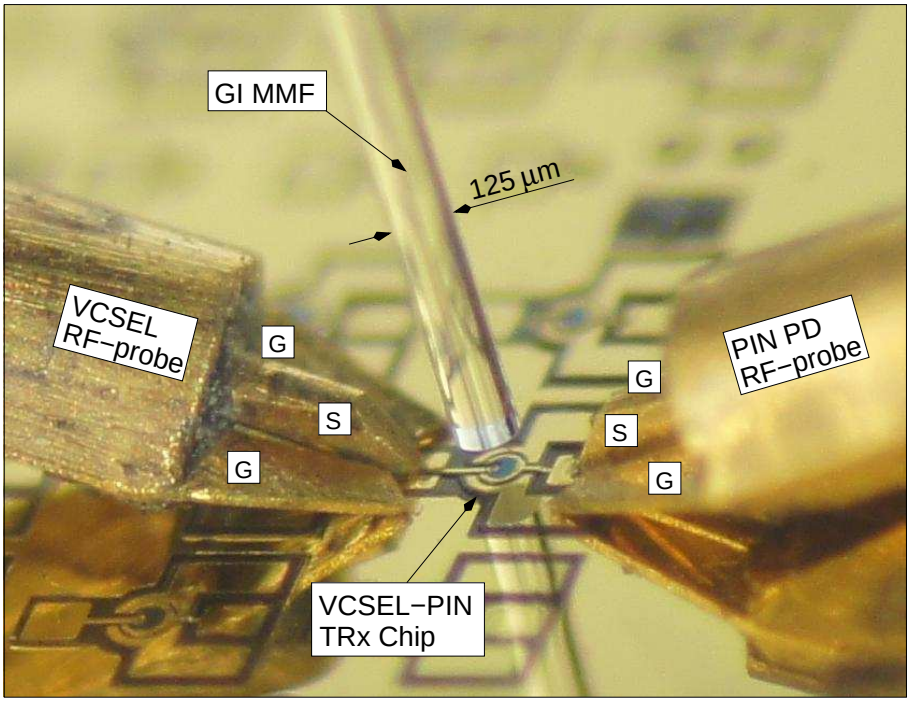

Fig. 1: Photograph of an on-wafer tested VCSEL–PIN transceiver chip butt-coupled to a standard MMF. The TRx chip is contacted with two ground–signal–ground (GSG) microwave probes for high-speed operation.

current is 1.2 mA, the maximum output power at thermal rollover is 4.5 mW at 12 mA injection current, and the slope efficiency amounts to 0.51 W/A at 5.9 mA bias current and room temperature. Taking the emission wavelength of around 823 nm at the same bias current and ambient temperature into account (see the inset in Fig. 2), a relatively low differential quantum efficiency of around 34 % is obtained. The short emission wavelength of the VCSEL originates from a VCSEL position far away from the center of the wafer, where the layers are thinner due to inhomogeneous growth by molecular beam epitaxy (MBE). As can be seen from the continuous increase of the threshold current with temperature, the cavity modes have shorter wavelengths than the gain peak even at room temperature. In other words, the VCSEL has negative detuning. In an improved device generation, positive detuning should be chosen, which will benefit the high-temperature characteristics of the device. A red-shift of the emission wavelength of around 4 nm in the inset of Fig. 2 occurs over 60 °C temperature increase, which corresponds to a well-known wavelength shift of approximately 0.065 nm/K induced by the refractive index change of the AlGaAs/GaAs materials [4]. At the same time, the threshold of the VCSEL increases by 1 mA and the maximum output power at rollover drops by 2.5 mW. Also the differential quantum efficiency at 80 °C drops to 20 % at 5.9 mA. The differential resistance extracted by linear interpolation of the current–voltage curve at high operating currents is 116 Ω and is almost constant with temperature.

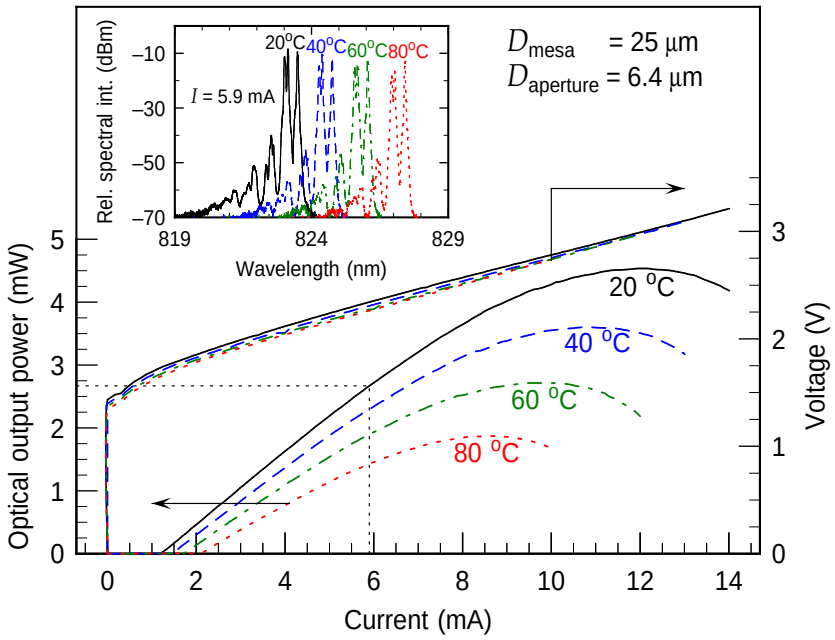

Fig. 2: Continuous-wave light–current–voltage characteristics of a TRx VCSEL for different ambient temperatures. The inset shows multimode emission spectra at a laser current of $I = 5.9\,\mathrm{mA}$ with a characteristic shift towards longer wavelengths for higher temperatures.

2.2 Transceiver PIN photodiode

For evaluation purposes, three different samples were grown, containing an identical epitaxial VCSEL structure but 1, 2, and 3 µm thick i-GaAs absorption regions of the PIN photodiode. Due to different chip topographies of up to several micrometers, more polyimide planarization steps had to be applied for thicker PDs. All three transceiver samples were anti-reflection-coated with a quarter-wave Al_2O_3 layer for 850 nm incident light, thus reducing the reflectivity at the semiconductor surface from initially approximately 30 % to 1.3 % over a spectral width of nearly 50 nm [5]. After the first transmission through the i-GaAs, the VCSEL structure underneath the photodetector leads to back-reflection of the non-absorbed portion of the incident light and thus to double-pass absorption. The increase of the responsivity and quantum efficiency for 1 µm thick PDs was reported in [6]. As can be seen in Fig. 3, the measured responsivity of a PIN photodiode with 2 µm thick absorption region is 0.66 A/W for an incident wavelength of $\lambda = 858\,\mathrm{nm}$ and thus nearly 16 % higher compared to a 1 µm PD with 0.57 A/W. This corresponds to 95 % and 82 % quantum efficiency, respectively. Unfortunately, the responsivity of the photodiode with 3 µm thick GaAs absorption layer is only 0.62 A/W, which corresponds to a quantum efficiency of 90 %. The relatively low value arises from the detuned VCSEL structure for the given sample. The reflectivity of the underlying DBR pair is only about 40 % at the measured incident light wavelength of 858 nm. Therefore only a reduced portion of the reflected light can be absorbed in the PD. Taking an absorption coefficient of $9000\,\mathrm{cm}^{-1}$ for high-purity GaAs at around 850 nm [7] and ideal reflection of the VCSEL stop-band into account, a maximum responsivity of 0.68 A/W and thus a quantum efficiency of 98 % is theoretically achievable for a 3 µm thick PIN PD.

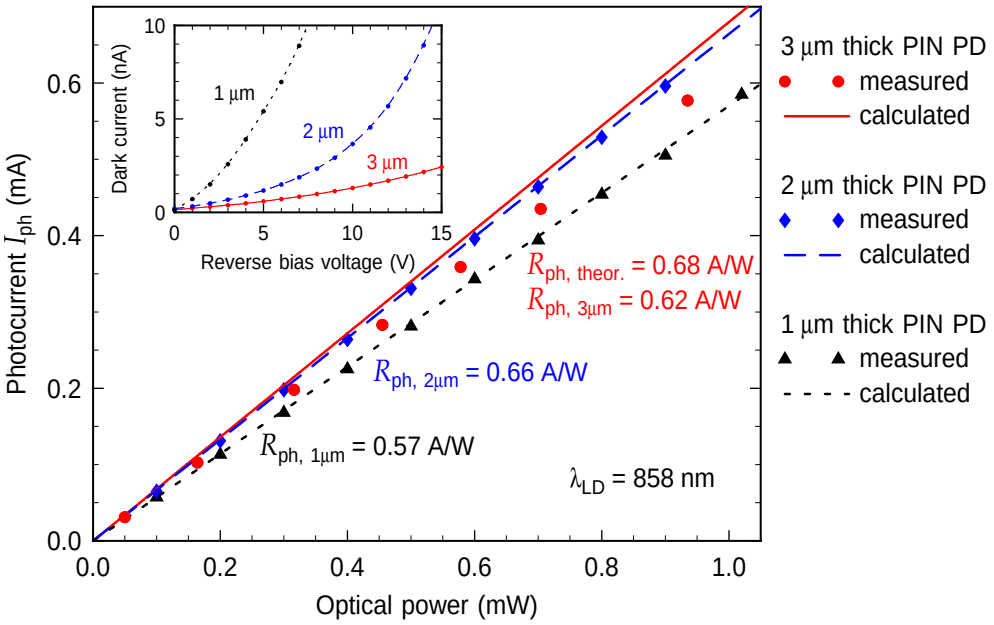

Fig. 3: Comparison of the measured (symbols) and calculated (lines) responsivities of integrated transceiver PIN PDs for samples with 1, 2, and 3 µm thick absorption regions for a laser emission wavelength of 858 nm. The inset shows the dark current behavior of PIN devices with different thicknesses for the reverse bias voltage range from 0 to 15 V.

The inset in Fig. 3 shows the dark current dependence of the three different PIN PDs with respect to the applied reverse bias voltage. Comparing the dark currents for identical values of the electric field strength in the absorption region, i.e., 3 V for 1 µm, 6 V for 2 µm, and 9 V for 3 µm thick PDs, it is < 2 nA for all photodetectors. The main reason for the exponential growth of the dark current is the increasing tunneling probability of the carriers due to stronger band bending for higher reverse bias voltages [4]. For optical data transmission experiments, the noise attributed to dark current can be neglected within the range of applied operating voltages.

3. Crosstalk Behavior of the Transceiver Chips

In this section we investigate the electrical and optical crosstalk in the closely integrated devices, which is important for full-duplex operation.

3.1 Electrical crosstalk

After the separate electro–optical as well as purely electrical characterization of the transmitter (Tx) and receiver (Rx), it is also necessary to investigate the mutual influence of the VCSEL and PIN PD, leading to a higher noise level in full-duplex mode operation of the transceiver chip. Owing to the very dense monolithic integration of the Tx and Rx, one might expect that a portion of the electrical power is coupled from the VCSEL

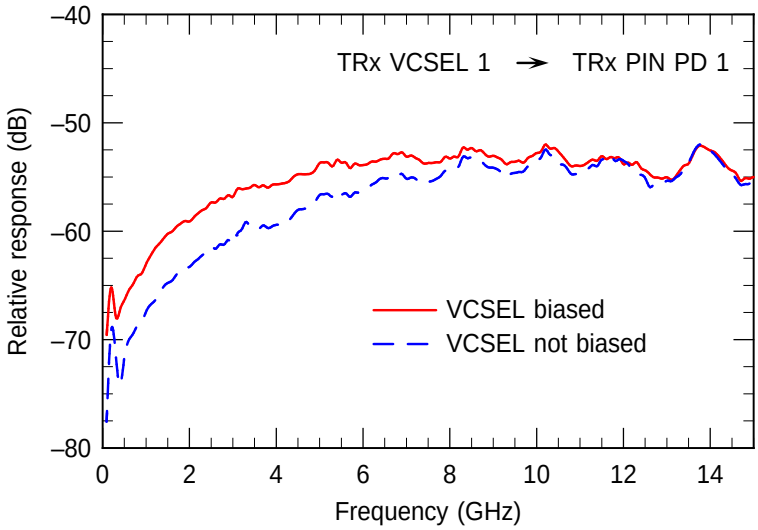

Fig. 4: Small-signal frequency response curves of electrically induced crosstalk between a VCSEL and a PIN PD of the same transceiver chip.

to the photodetector. In the experiment, a solitary TRx chip was contacted by two microwave probes as in Fig. 1, however, without the fiber in place. The VCSEL is driven by a low-power modulating signal generated by a sweep oscillator. On the PD side, the coupled electrical power is measured by an electrical spectrum analyzer. Figure 4 shows the frequency responses as ratios of both signals for a biased and unbiased state of the VCSEL. Both curves indicate a high-pass characteristic starting from around −70 dB coupling for MHz frequencies and increasing to values still well below −50 dB for frequencies between 8 and 15 GHz. Thus, the contribution to the system noise originating from electrical crosstalk is negligible. Nevertheless, at lower frequencies, the crosstalk for a biased VCSEL is up to 5 dB higher compared to VCSEL operation below threshold. The higher values can be attributed to optical crosstalk between VCSEL and PIN PD, where a small portion of the emitted light is directly detected by the photodetector. This is discussed in more detail in the following subsection. As expected, the difference vanishes for high frequencies above the bandwidth of the PD.

3.2 Optical crosstalk

Although VCSEL and PIN PD are densely integrated, both devices are electrically isolated by a narrow, deep trench. Therefore the electrical crosstalk was expected to be very low. However, optical crosstalk can also lead to a bandwidth trade-off in full-duplex mode operation. Inspecting the schematic of a MMF butt-coupled TRx link in Fig. 5, we can identify two main sources of optical crosstalk, namely the reflections of the emitted light at the near and far ends of the fiber as well as at the opposite TRx chip. Additionally, as already mentioned in the previous subsection, there is direct light detection by the integrated photodetector. In Fig. 6, the amount of static optical crosstalk is presented as a function of the optical power of one of the VCSELs. The measurements were performed in the transmission direction from chip 2 to chip 1. We thus detect the optical crosstalk of

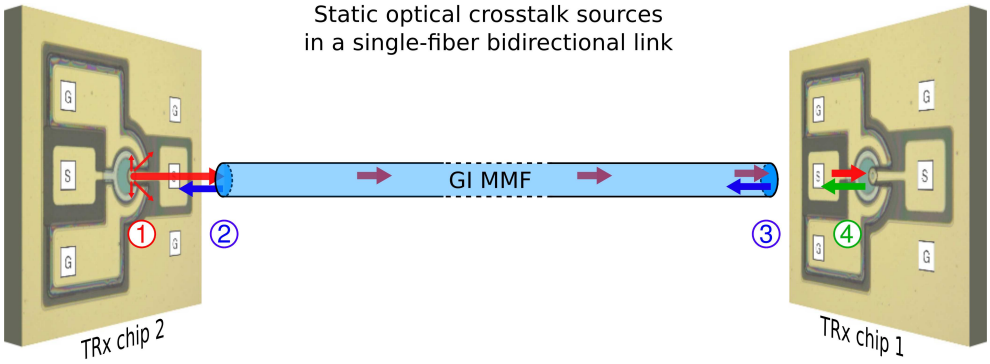

Fig. 5: Schematic illustrating the four origins of optical crosstalk for chip 2 in half-duplex operation of a data link from chip 2 to chip 1.

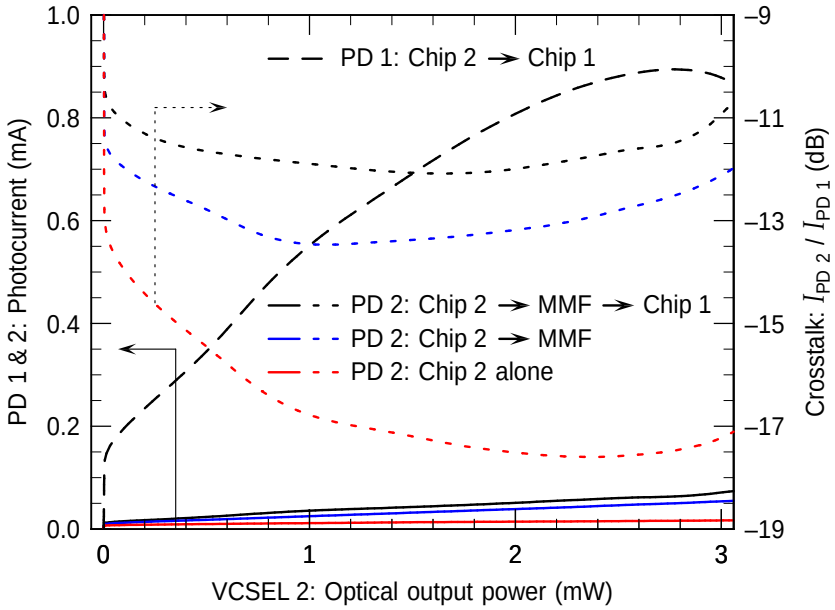

Fig. 6: Static optical crosstalk sources for chip 2 (solid and dotted) compared to the transmitted signal power to chip 1 (dashed) in a butt-coupled single-fiber bidirectional transceiver link.

PD 2 originating from VCSEL 2. For comparison, the transmitted signal power detected by PD 1 is plotted as black dashed line. Its slope decreases with higher laser power. The probable underlying reason is the changing beam profile and thus lower fiber coupling efficiency of the multimode VCSEL with higher laser current.

In the first step, similar to the measurement of electrical crosstalk in the previous subsection, the solitary TRx chip 2 was operated. Here, only direct current (DC) but no modulation was applied to VCSEL 2. The optical crosstalk then arises from the spontaneous emission of the VCSEL. Carrier clamping prevents a significant increase of photocurrent 2 (red solid line) for higher output powers. The red dotted line in Fig. 6 refers to the vertical axis on the right and quantifies the amount of optical crosstalk over the received optical power at the opposite PD 1. Here, for the common operating regime of VCSEL 2, it is about 17 dB below the signal power and thus nearly negligible.

In the second step, a 5 m long MMF was butt-coupled (about 30 µm distance) to TRx chip 2. The measured optical crosstalk (blue solid line) now originates additionally from the reflections at both fiber ends. In Fig. 6 (blue dotted line), the crosstalk increases by 4–5 dB.

Finally, TRx chip 1 was coupled to the other end of the MMF. The photocurrent of PD 2 (black solid line) increases by approximately another 1 dB due to the reflections at the opposite chip 1. Thus, the total amount of optical crosstalk power (black dotted line) is at least 11 dB below the transmitted signal power (black dashed line). It is important to mention that the total amount of optical crosstalk is dependent on the alignment of the MMF to the TRx chips and might vary from chip 1 to 2.

4. MMF–TRx Chip Alignment Tolerances

Due to the fact that VCSEL and PIN PD are butt-coupled to a single MMF without any use of external optics, it is essential to investigate the allowed fiber misalignment. The inherent misalignment of the VCSELs to the fiber core influences the optical crosstalk and the achievable bandwidth in both, half- and full-duplex mode.

For the measurement of the Rx detection efficiency, a VCSEL was coupled to the far end of a GI MMF with 50 µm core diameter, whereas the near end was mounted on a computer-controlled translation stage with an adjustment tolerance of < 1 µm. The coupling efficiency of the Tx was determined in the opposite way by coupling a TRx VCSEL to the moveable near end of the MMF and detecting the transmitted optical power at the far end. For the sake of simplicity, we chose the center of the VCSEL aperture in the TRx chip as the origin of a coordinate system. For both experiments, the initial position of the fiber core was at $x_0 = -18$ µm, $y_0 = 0$, as indicated by the solid circles in Fig. 7. In this position, the near end of the MMF is $z_0 = 30$ µm away from the TRx chip surface in order to prevent an etalon effect.

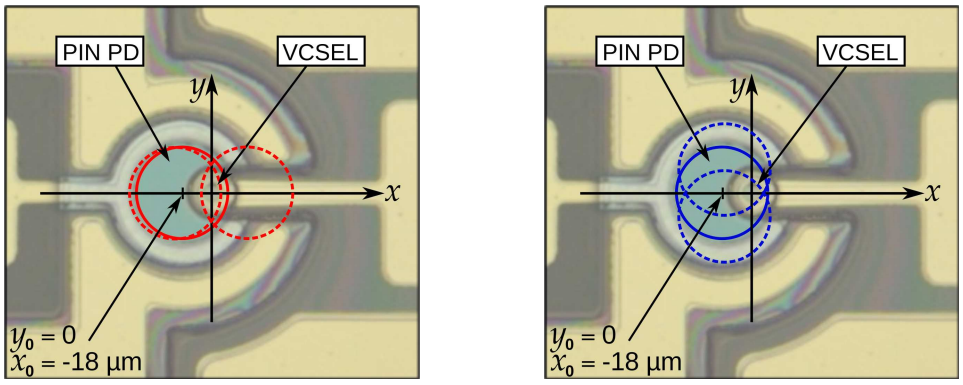

Fig. 7: Photograph of a TRx chip with positions of the 50 µm diameter fiber core for misalignments in x- (left) and y-directions (right). The dashed circles indicate the maximum possible fiber misalignment for VCSEL–fiber coupling and the solid circles show the optimum alignment at x_0 and y_0 for bidirectional data transmission experiments.

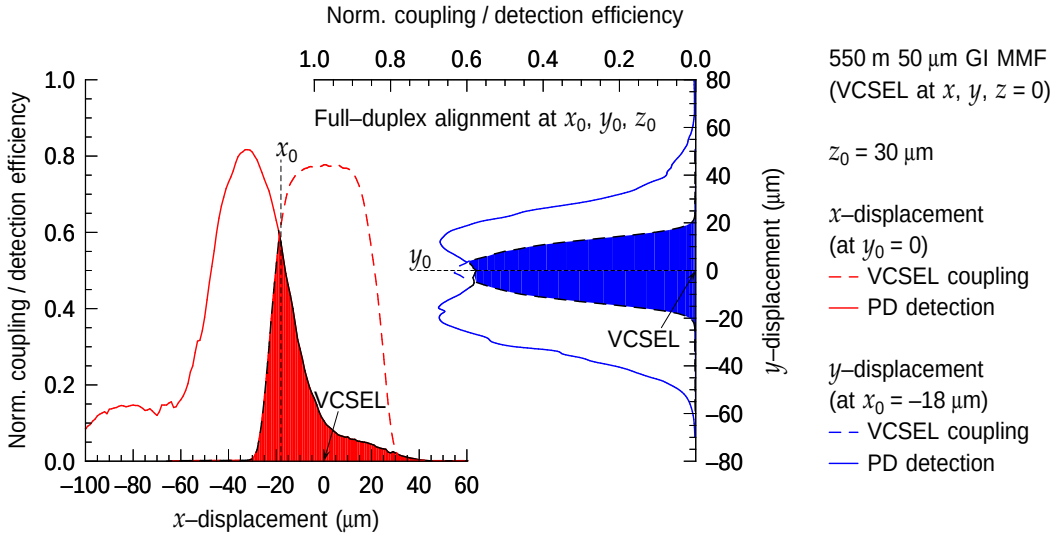

Fig. 8: Measurement of VCSEL–fiber coupling (dashed) and photodetector detection efficiency (solid) in a single-fiber bidirectional link for x- (red) and y-displacement (blue) of a butt-coupled MMF with about $z_0 = 30\,\mu\text{m}$ distance.

In the first step, the fiber was moved along the y-direction at $x_0 = -18\,\mu\text{m}$. In Fig. 8 the detection efficiency of the photodetector reaches maximum values of ~ 0.65 at $y = \pm 15\,\mu\text{m}$ (blue solid line), where the fiber core has the best overlap with the PD area. An efficiency of 1 is only possible with full-area circular photodiodes in which the photoactive area is not partly occupied by a VCSEL. A coupling efficiency of 0.6 is measured for the VCSEL at y_0, with a strong decrease when the fiber is moved away from the initial position (blue dashed line). The maximum possible y-misalignment range is indicated in Fig. 7 (right) by two blue dashed circles. Therefore in y-direction, the maximum achievable alignment tolerance is limited only by the coupling efficiency of the VCSEL as illustrated by the blue shaded area in Fig. 8. The full-width at half-maximum (FWHM) is 26 µm ($y \approx \pm 13\,\mu\text{m}$).

In the second step, the near end of the fiber was moved along the x-axis at $y_0 = 0$. Since the VCSEL is positioned 18 µm off-center in the x-direction with respect to the PD, the curves for the detection and coupling efficiencies are also displaced. Here, maximum efficiencies of ~ 0.8 can be achieved for each individual device. However, the combined maximum efficiency is ~ 0.6. Although the curve for the coupling efficiency of the VCSEL (red dashed line in Fig. 8) is wider compared to the measurement in y-direction, the allowed displacement for the PD detection (red solid line) is narrower. The overlap of both measurements, indicated by the red shaded area in Fig. 8, defines the alignment tolerance with a FWHM of 14 µm ($x \approx \pm 7\,\mu\text{m}$). Therefore misalignments in x-direction are more critical compared to the y-direction.

In summary, the optimal MMF–TRx chip alignment is a compromise between the VCSEL coupling efficiency and the PD detection efficiency. It is found at x_0, y_0 for the highest common values of the red and blue shaded areas in Fig. 8. In future, a centered (and ideally also smaller) TRx VCSEL which is surrounded by the PD would be an improvement regarding easier chip alignment, as already shown in [5] for VCSEL–MSM (metal–semiconductor–metal) TRx chips.

5. Conclusion

We have presented latest results on fully integrated 850 nm wavelength transceiver chips for single-fiber bidirectional optical data transmission. The chips consist of PIN photodiodes and oxide-confined, top-emitting VCSELs, integrated to match with butt-coupled 50 µm core diameter GI MMFs.

PIN PDs with an intrinsic absorption region thickness of 3 µm show dark currents below 2 nA and an estimated quantum efficiency of nearly 98 % for an optimum Bragg mirror design. Those PDs also have highest 3-dB bandwidths of around 8 GHz. The maximum small-signal bandwidth of the VCSEL is 12.5 GHz and thus the highest operation data rate of the transceiver chip is limited by the PIN PD. The dynamic characteristics were not reported here.

We have investigated the crosstalk properties of the integrated devices, since they affect the data transmission in full-duplex mode. The optical crosstalk is 11 dB below the signal photocurrent level and originates from the reflections at both fiber ends and at the opposite TRx chip as well as from spontaneous emission of the adjacent VCSEL. The electrical crosstalk between VCSEL and PIN PD of the same chip is attenuated by around 50 dB and can be rather neglected.

Fiber alignment tolerances along the chip surface have been determined to be around ±7 µm and ±13 µm in orthogonal directions. Further miniaturization of the VCSEL and its monolithic integration in the center of the PD would increase the alignment tolerances as well as the fiber coupling of the VCSEL.

The demonstrated monolithic transceiver design based on a well-established material system is well suited for low-cost and compact optical links over distances of a few hundred meters. Capable to handle data rates of up to 10 Gbit/s, these transceiver chips can be employed, e.g., to upgrade existing standard multimode fiber networks to bidirectional operation.

Acknowledgment

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Surface Grating Optimization for Low-Threshold Atomic Clock VCSELs

Md. Jarez Miah, Ahmed Al-Samaneh, and Pierluigi Debernardi

Vertical-cavity surface-emitting lasers (VCSELs) with emission in a single-mode, single-polarization beam at a wavelength of 894.6 nm have been fabricated for use in Cs-based atomic clocks. For polarization control, monolithically integrated surface gratings are employed. Simulated and experimental results show that the longitudinal position of the surface grating has a significant influence on the threshold current. With a grating in the topmost in-phase layer, the threshold currents are reduced to 40 % compared to earlier atomic clock grating VCSELs with inverted structure. The output polarization is parallel to the grating lines with a peak-to-peak difference between the dominant and the suppressed polarization modes of 25 dB even at substrate temperatures up to 80° C. Small-signal modulation characteristics of grating VCSELs are presented. The modulation bandwidth exceeds the required 5 GHz at a bias current of only 0.9 mA above threshold at room temperature.

1. Introduction

Owing to their low power consumption, high modulation bandwidth, and favorable beam characteristics, VCSELs are compelling light sources for miniature atomic clocks [1]. Similar to the use in tunable laser absorption spectroscopy for regular gas sensing, they must feature strictly polarization-stable single-mode emission. Additionally, they must provide narrow linewidth emission at a center wavelength of about 894.59 nm and be well suited for harmonic modulation at about 4.6 GHz in order to employ the coherent population trapping effect at the cesium D1 line [2].

Polarization stability of VCSELs is most conveniently achieved with an integrated linear semiconductor surface grating [3]. A schematic drawing of a surface grating etched in the topmost layer of the upper Bragg mirror of a VCSEL is shown in Fig. 1. The grating can be integrated in a standard VCSEL structure with very little additional processing effort and thus low cost and can be designed such that there is no penalty for laser characteristics like threshold current, differential efficiency, or far-field emission profile. Insensitivity to optical feedback and external stress has also been proven. The results are documented in a series of publications which are summarized in [3, 4]. It is worth to note that the grating-based polarization control technique was commercialized very soon after its invention and is applied today in a large fraction of 850 nm wavelength VCSEL sensors in optical navigation devices like computer mice [5, 6]. Our present work on VCSELs for Cs-based miniature atomic clocks also relies on such pure semiconductor–air surface gratings [7, 8]. In particular, so-called inverted grating VCSELs have been employed [9],

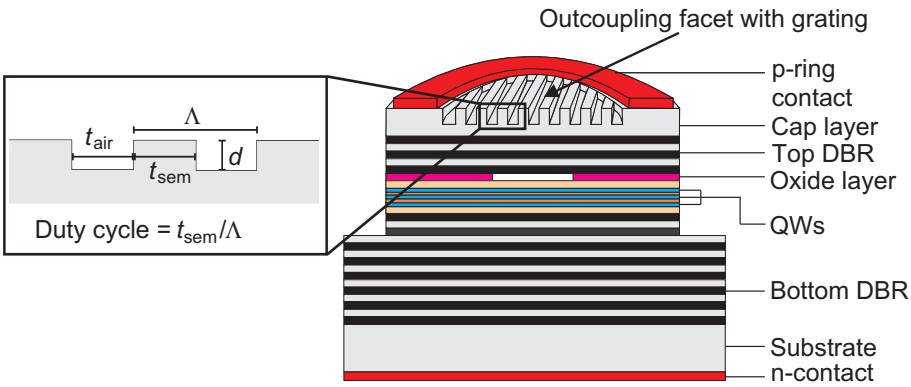

Fig. 1: Illustration of a surface grating VCSEL (right) and various grating parameters (left). Λ is the grating period, d is the grating etch depth, t_{air} and t_{sem} are the width of the grating groove and ridge, respectively.

where the grating is etched in an extra topmost GaAs quarter-wave antiphase layer. An alternative approach to full-area gratings is to etch a surface grating over a circular area of only 3 to 4 µm diameter in the center of the outcoupling facet. Such inverted grating relief VCSELs simultaneously provide favorable single-mode and single-polarization emission [10]. However, inherently higher optical losses, even of the fundamental mode, lead to larger threshold currents compared to regular inverted grating VCSELs. In this article we investigate the use of a different type of surface grating which is etched in an extra topmost half-wave GaAs in-phase layer, referred to as normal grating VCSELs. It provides lower threshold operation that is much desired for low-power atomic clock applications.

2. VCSEL Design and Fabrication

The VCSEL layers are grown on n-doped (100)-oriented GaAs substrates using solid-source molecular beam epitaxy. There is a highly n-doped GaAs contact layer above the GaAs substrate to allow n-contacting. Emission at 894.59 nm wavelength is efficiently achieved with three compressively strained 8 nm thick $In_{0.04}Ga_{0.96}As$ quantum wells (QWs) separated by 10 nm thick $Al_{0.27}Ga_{0.73}As$ barrier layers. The active region is sandwiched between two larger bandgap $Al_{0.47}Ga_{0.53}As$ cladding layers to form a one-wavelength thick inner cavity. A highly p-doped 30 nm thick AlAs layer is positioned at the node of the standing-wave pattern above the inner cavity. It is wet-thermally oxidized after mesa etching to achieve current confinement and optical index guiding. The n-type bottom and p-type top DBRs consist of 38.5 Si-doped and 25 C-doped $Al_{0.90}Ga_{0.10}As/Al_{0.20}Ga_{0.80}As$ layer pairs, respectively. The DBRs are graded in composition and doping concentration to minimize the free-carrier absorption and decrease the electrical resistance. The structure has an extra topmost GaAs cap layer in which the surface grating for polarization control is etched. The thickness of the cap layer is three quarter-wave (which is equivalent to one quarter-wave) or half-wave to construct inverted or normal VCSEL structures, respectively. In order to avoid diffraction losses in air, gratings with sub-wavelength periods of 0.6 µm and 50 % duty cycle are employed in both VCSEL types. The grating lines are etched along the [011] crystal axis, which,

resulting from the electro-optic effect, is one of the two preferred orthogonal polarization directions of standard GaAs VCSELs [3]. In the remaining part of this section, we discuss the optimization of the QW composition, the grating depth and its longitudinal position, as well as the p-DBR mirror thickness.

2.1 Active region

VCSELs to be incorporated in miniaturized atomic clock microsystems experience elevated temperatures of usually $T = 65$ to 80°C. Thus, for optimization of the active region, an experimental study with different indium content x in the $In_xGa_{1-x}As/Al_{0.27}Ga_{0.73}As$ QWs has been performed. A higher x reduces the bandgap energy and thus shifts the optical gain spectrum to longer wavelengths. Consequently, x changes the alignment between the cavity resonance (or emission wavelength) and the gain peak and hence the temperature at which the threshold current is minimized. The threshold currents of three VCSELs with different x but identical resonance wavelengths at room temperature are illustrated in Fig. 2 as a function of T. For constant x, the change of threshold current with temperature can be attributed mainly to the change of the material gain itself and the change of detuning between cavity resonance and gain peak, whereas the mirror reflectivities remain almost constant. One VCSEL has $x = 6\,\%$ and $N_p = 25$ top Bragg mirror pairs. It exhibits a minimum threshold at around 20°C. By reducing x to 4.5 % and 4 %, the point of minimum I_{th} is shifted to around 55°C and 75°C, respectively. The latter has a minimum I_{th} within the operating range of the atomic clocks. Therefore, QWs with 4 % In content have been employed in the VCSELs reported below. The magnitude of I_{th} depends on x, N_p, the active diameter as well as the presence or absence of a surface grating. The main concern of the experiments summarized in Fig. 2, however, was to optimize the point of minimum I_{th}.

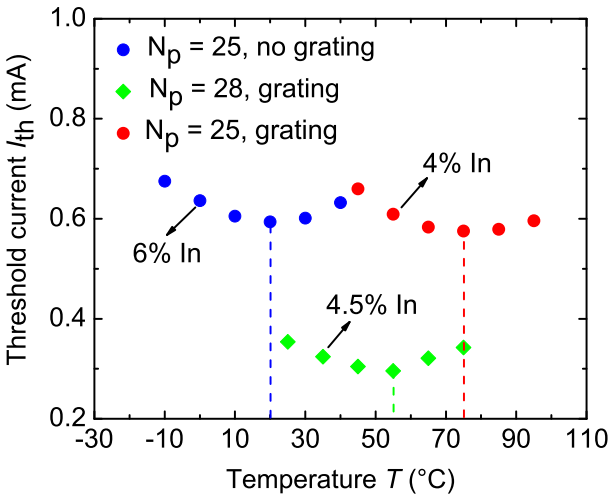

Fig. 2: Temperature dependence of the threshold current of three VCSELs with quantum wells having 6 %, 4.5 %, and 4 % indium content. The first device has 4 µm active diameter, the other two 4.5 µm. The VCSELs emit at approximately 894 nm wavelength at room temperature. They differ in the number of top mirror pairs N_p and the presence of a surface grating.

2.2 Longitudinal position of the grating

Simulations of the layer structure of 894.59 nm atomic clock VCSELs have been done using a fully vectorial, three-dimensional model based on coupled-mode theory [11, 12]. It very

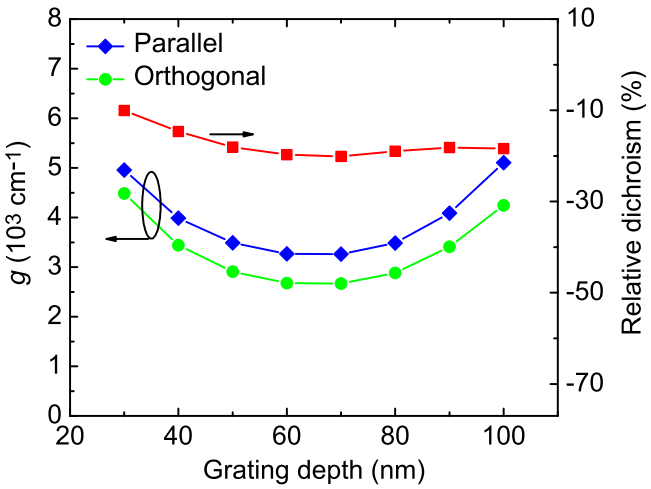

Fig. 3: Simulated material threshold gains g of the two fundamental polarization modes at $T = 20°C$ as a function of the grating depth of an inverted grating VCSEL (left axis) and the corresponding relative dichroism calculated from the threshold gains using $\mathrm{RD} = (g_{\mathrm{orth}} - g_{\mathrm{par}})/(0.5\,(g_{\mathrm{orth}} + g_{\mathrm{par}}))$ (right axis). The laser has 4 µm active diameter and $N_{\mathrm{p}} = 25$. The surface grating has 0.7 µm period and 50 % duty cycle.

well predicts the cold-cavity properties of VCSELs even with non-circular geometry [13]. Simulation results are the modal emission wavelengths, the material threshold gains of the polarization modes, as well as their field distributions. For an inverted grating VCSEL with 0.7 µm grating period and 50 % duty cycle, Fig. 3 depicts the dependence of the material threshold gains of the two fundamental transverse modes polarized parallel and orthogonal to the grating lines for grating depths d varied between 30 and 100 nm. The relative dichroisms calculated from the threshold gains are also plotted in the figure. A negative relative dichroism is observed over the whole range of grating depths, which indicates that the VCSEL emission is polarized orthogonal to the grating lines. In order to have the lowest threshold gain and hence the minimum threshold current, d should be around 70 nm, which is about one quarter of the material wavelength.

The corresponding simulation results for a normal grating VCSEL with the same active diameter, grating period, and duty cycle are depicted in Fig. 4. For grating depths below 42 nm, the threshold gain of the parallel polarization mode is larger than that of the orthogonal polarization. The situation is reverse for larger grating depths. Thus, the relative dichroism changes its sign from negative to positive at $d_{\mathrm{c}} = 42$ nm, favoring the parallel polarization for $d > d_{\mathrm{c}}$. Figure 4 shows that the material threshold gain of the selected polarization mode is minimum at around 130 nm or about half material wavelength grating depth. The minimum threshold gain is approximately 30 % of the corresponding minimum of the inverted grating VCSEL at $d = 70$ nm in Fig. 3. Reduced threshold currents of normal grating VCSELs are thus expected. The experimentally obtained I_{th} of several inverted grating and normal grating VCSELs having different active areas are displayed in Fig. 5. Both normal and inverted grating VCSELs have 0.6 µm grating period and 50 % duty cycle, however, $d = 120$ nm and 70 nm for normal and inverted grating VCSELs, respectively. Normal grating VCSELs in the lower ellipse

in Fig. 5 show an average I_{th} of about 0.2 mA, which is approximately 40 % of the I_{th} of the inverted grating VCSELs in the upper ellipse within the same range of active areas between 5 to 10 µm^2.

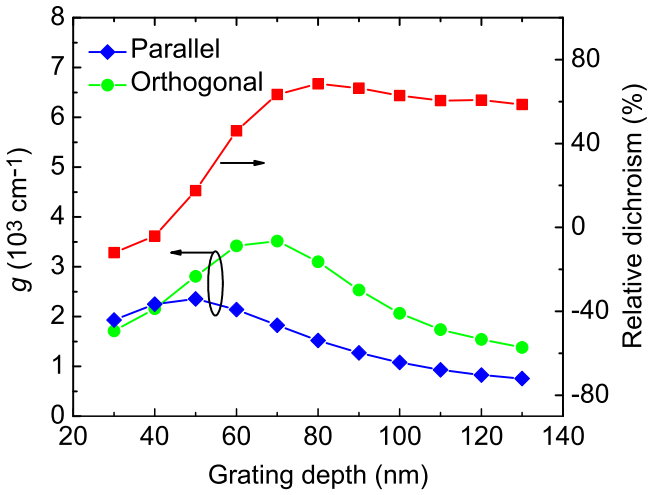

Fig. 4: Simulated material threshold gains and relative dichroism with all parameters as in Fig. 3, here for a normal grating VCSEL.

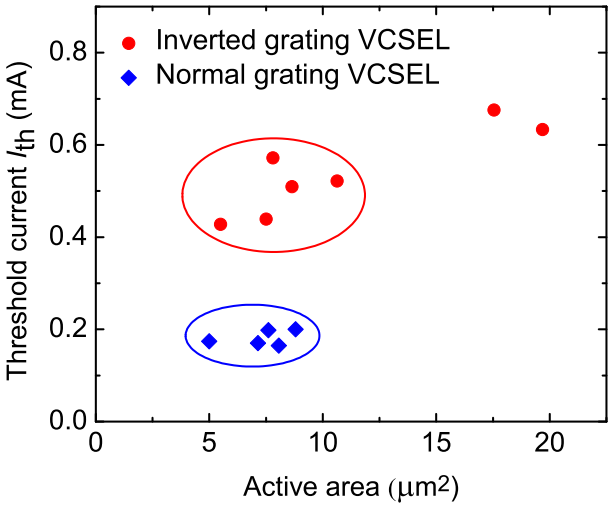

Fig. 5: Experimentally obtained threshold currents of seven inverted grating VCSELs and five normal grating VCSELs with different active areas. Inverted and normal grating devices with a similar range of active areas are grouped in two ellipses. $N_{\mathrm{p}} = 25$ and $T = 20$°C for all VCSELs.

2.3 Outcoupling mirror

A major trade-off in designing grating VCSELs are the material threshold gain and the relative dichroism achieved with different numbers of layer pairs of the outcoupling mirror. Figure 6 (top) illustrates the simulated material threshold gains of the two fundamental modes polarized parallel and orthogonal to the grating lines in dependence of the grating depth for different N_{p} of the normal grating VCSEL from Fig. 4. With increasing N_{p}, the threshold gains decrease due to the increased reflectivity of the top Bragg mirror. On the other hand, there is a lower field intensity at the surface grating (i.e., the surface grating

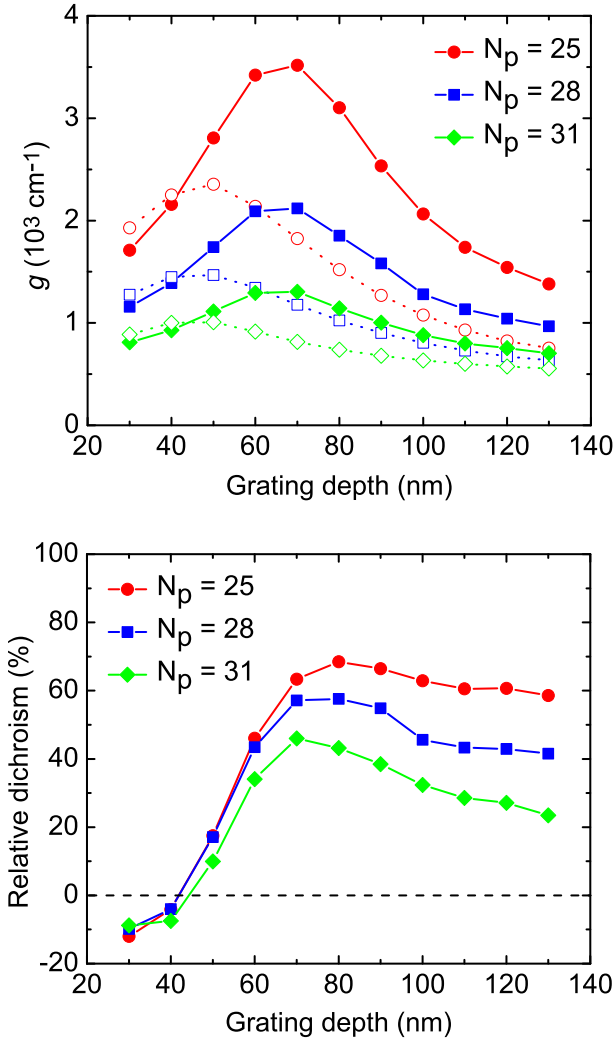

Fig. 6: Simulated material threshold gains of the two fundamental polarization modes as a function of grating depth of the normal grating VCSEL structure from Fig. 4 for different numbers of top Bragg mirror pairs N_p (top) and the corresponding relative dichroisms (bottom). The full and open symbols in the top figure represent the material threshold gains of the two fundamental modes polarized orthogonal and parallel to the grating lines, respectively.

is more decoupled from the laser cavity) and thus its polarization control effect becomes weaker. This trend is reflected in the relative dichroism which decreases with increasing N_p, as depicted in Fig. 6 (bottom). Polarization stability is a high priority for atomic clock VCSELs, to be ensured under all adverse operating conditions like high-frequency modulation or possible optical feedback in the clock microsystem. To be on the very safe side, we have limited the number of top Bragg mirror pairs in this study to 25. A higher N_p might still provide sufficient polarization stability in practice, with the benefit of further reduced I_th and higher insensitivity to optical feedback. The available output power which decreases with higher N_p is not a major concern since the clock does not require more than 100 µW. At this point, it is not possible to identify a strict upper limit for N_p.

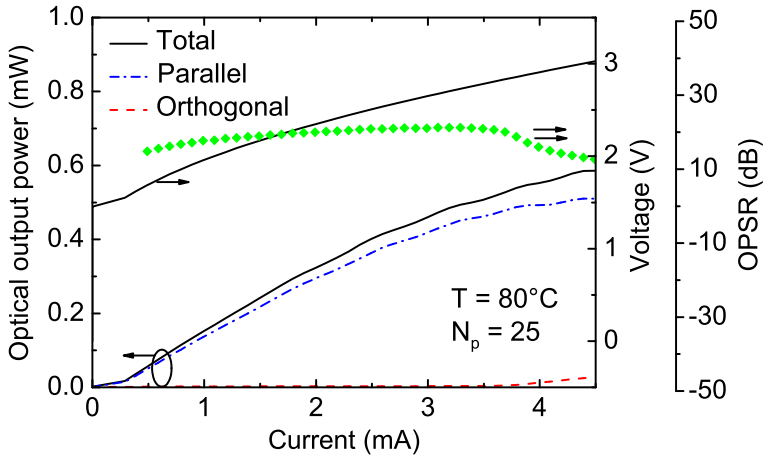

Fig. 7: Polarization-resolved operation characteristics of a normal grating VCSEL with 3 µm active diameter at 80°C substrate temperature. The grating has 0.6 µm period and 120 nm depth.

3. Experimental Results

3.1 Static characteristics

As mentioned earlier, VCSELs in Cs-based atomic clocks are exposed to temperatures T of typically 80°C. Therefore we have chosen this temperature for VCSEL characterization in the present section. Figure 7 depicts the polarization-resolved light–current–voltage (PR-LIV) characteristics of a normal grating VCSEL with an active diameter of 3 µm, a grating period of 0.6 µm and a grating depth of 120 nm. The optical powers of the two polarization modes are measured behind a Glan–Thompson polarizer by orienting its transmission direction parallel and orthogonal to the grating lines. The corresponding powers are denoted as P_{par} and P_{orth}. They are indicated in the figure by dash-dotted and dashed lines, respectively. The losses of the polarizer are responsible for the total power in Fig. 7 being larger than $P_{\mathrm{par}} + P_{\mathrm{orth}}$. The orthogonal polarization suppression ratio (OPSR) is calculated from the ratio of the two powers as $\mathrm{OPSR} = 10\log(P_{\mathrm{par}}/P_{\mathrm{orth}})$ and is displayed in the figure with green symbols. The VCSEL remains polarization-stable from its threshold current of approximately 0.2 mA up to thermal roll-over with an average OPSR of 19 dB and a peak value of 21 dB. The average OPSR is calculated from the data for currents in steps of 0.1 mA and output powers corresponding to 10 . . . 100 % of the maximum. Figure 8 shows the polarization-resolved high-temperature spectra. The target wavelength of 894.59 nm is reached at a bias current $I = 1.8$ mA with a side-mode suppression ratio (SMSR) of 42 dB. The peak-to-peak difference between the dominant and the suppressed polarization modes is about 25 dB. Both the SMSR and the peak-to-peak difference between the dominant and suppressed polarization modes far exceed the target values of 20 dB. The dominant polarizations of the normal grating VCSELs are always found to be parallel to the grating lines, which is consistent with the simulation results in Fig. 4 for about 120 nm grating depth. Figure 9 illustrates experimentally obtained average OPSRs of several normal and inverted grating VCSELs having 0.6 µm grating period. The normal and inverted grating VCSELs have 120 nm and 70 nm grat-

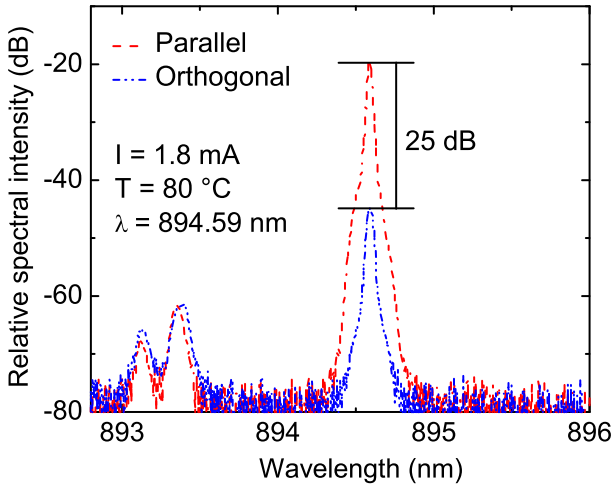

Fig. 8: Polarization-resolved spectra of the grating VCSEL from Fig. 7 at $I = 1.8\,\mathrm{mA}$ and $T = 80°\mathrm{C}$.

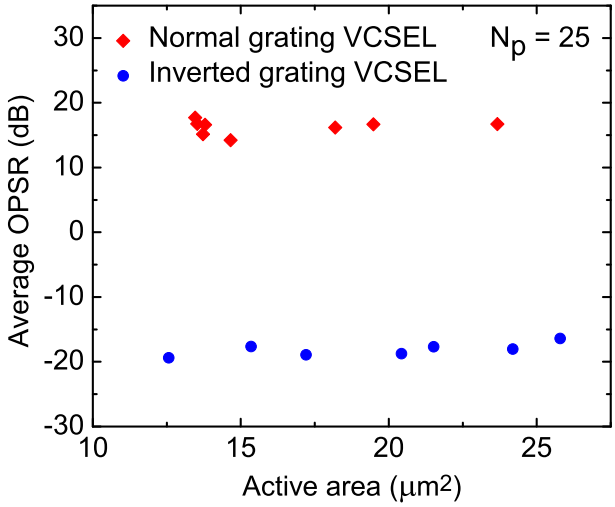

Fig. 9: Experimentally obtained average OPSRs of several normal and inverted grating VCSELs with different active areas at 80°C substrate temperature. The gratings have 0.6 µm period and 120 nm (70 nm) depth for normal (inverted) grating VCSELs.

ing depth, respectively. Positive OPSRs indicate the dominant polarization modes of the normal VCSELs to be parallel to the grating lines. In contrast, the dominant polarization of the inverted grating VCSELs is orthogonal to the grating, thus OPSR $< 0\,\mathrm{dB}$. It is worth noting that VCSELs in Fig. 9 with active areas larger than about $20\,\mu\mathrm{m}^2$ tend to be transverse multimode at higher currents. As is well known [3, 4], surface gratings also stabilize the polarization of higher-order modes.

3.2 Emission far-fields

The effect of the surface grating on the beam properties of normal grating VCSELs is investigated by measuring the emission far-fields. Figure 10 shows the far-fields parallel and

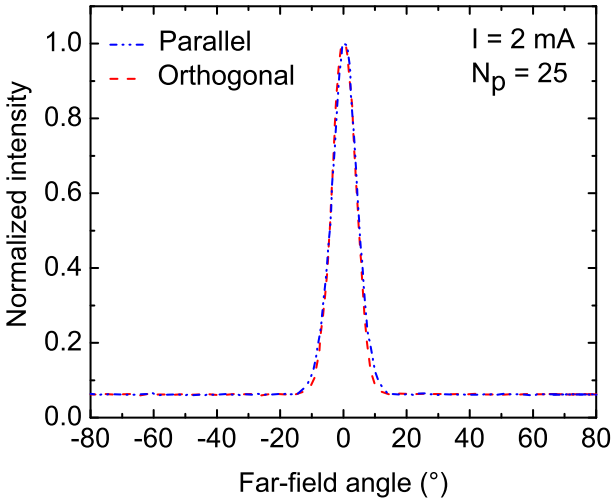

Fig. 10: Emission far-fields of a normal grating VCSEL with an active diameter of 4.8 µm, measured at $T = 20°C$. The almost overlapping dash-dotted and dashed lines indicate the normalized optical intensity parallel and orthogonal to the grating lines, respectively.

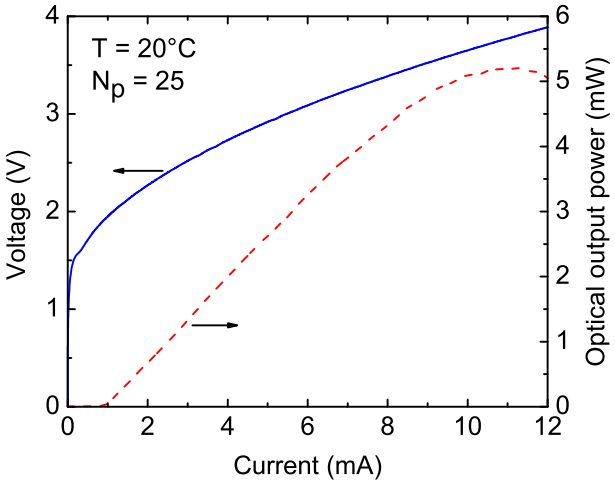

Fig. 11: LIV characteristics of a grating VCSEL with 5.3 µm active diameter.

orthogonal to the grating lines of a normal grating VCSEL with 4.8 µm active diameter at $I = 2\,\text{mA}$ and $T = 20°C$. The grating depth is 120 nm and the period is 0.6 µm. The absence of side-lobes in the emission far-fields proves that VCSELs with sub-emission-wavelength grating periods do not suffer from diffraction losses in air. Almost identical far-field patterns along the parallel and orthogonal directions indicate a circular beam profile. The Gaussian-like shape reflects the single-mode emission of the VCSEL at the given current.

3.3 Small-signal modulation response

Cs-based miniature atomic clocks require VCSELs with modulation bandwidths exceeding 5 GHz. The dynamic behavior of normal grating VCSELs is described in this section. The small-signal modulation responses are measured using a setup similar to the one described in [7]. LIV characteristics of a VCSEL with 5.3 µm active diameter are presented in Fig. 11 at $T = 20°C$. Figure 12 displays the small-signal modulation curves of the VCSEL at different bias currents. The threshold current is 0.90 mA. As usual it is observed that at higher bias currents, both the resonance frequency and the damping increase.

The maximum 3 dB bandwidth of 11.8 GHz is obtained at $I = 7.0$ mA. A bandwidth of 5.6 GHz, already exceeding the target value of 5 GHz, is obtained at $I = 1.8$ mA, i.e., only 0.9 mA above threshold.

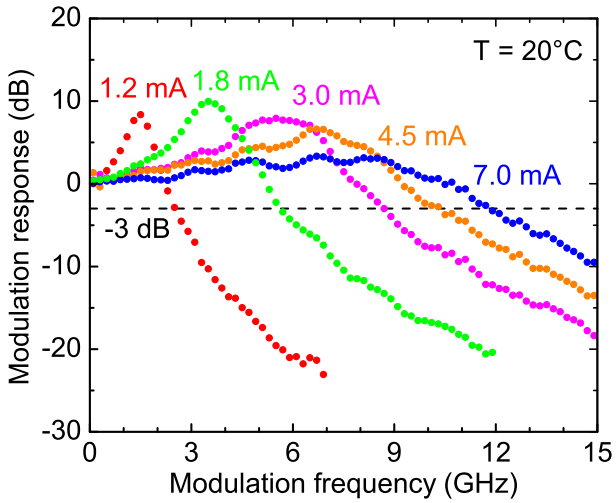

Fig. 12: Small-signal modulation response curves of the device from Fig. 11 at different bias currents and $T = 20$°C.

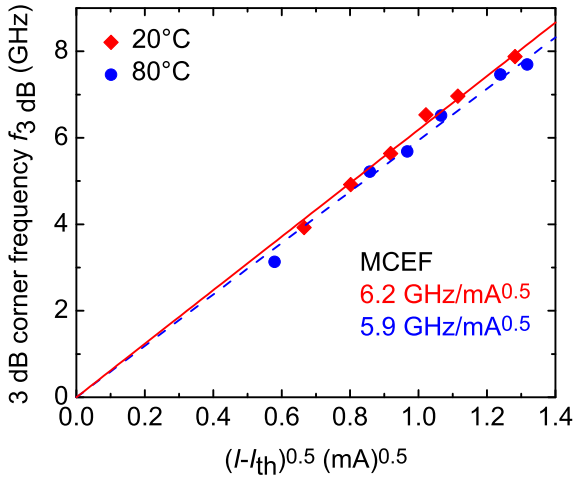

Fig. 13: 3 dB corner frequencies as a function of $\sqrt{I - I_{\mathrm{th}}}$ for the grating VCSEL from Figs. 11 and 12 at $T = 20$°C (solid) and 80°C (dashed). The MCEFs are determined from the slopes of the linear fits.

In order to determine the modualtion current efficiency factor (MCEF) defined as MCEF $= f_{3\,\mathrm{dB}}/\sqrt{I - I_{\mathrm{th}}}$, 3 dB corner frequencies $f_{3\,\mathrm{dB}}$ of the VCSEL are extracted from the small-signal modulation responses and plotted against $\sqrt{I - I_{\mathrm{th}}}$ in Fig. 13. Equivalent measurements of modulation responses and LIV characteristics of the same VCSEL were also performed at 80°C and the $f_{3\,\mathrm{dB}}$ are included in Fig. 13. The MCEFs are determined from linear fits. Values of 6.2 and 5.9 GHz/$\sqrt{\mathrm{mA}}$ are obtained at 20 and 80°C, respectively. The smaller MCEF at higher temperature is likely due to reductions of the current injection efficiency and the differential gain coefficient.

4. Conclusion

By simulations as well as experiments, we have shown that normal grating VCSELs have inherently lower threshold currents than equivalent inverted grating devices. Such low threshold, single-mode, and polarization-stable VCSELs emitting at 894.59 nm wavelength have been fabricated for use in Cs-based atomic clocks. The dynamic laser properties have been reported. The required modulation bandwidth of 5 GHz is reached close above threshold. These optimized VCSELs are very well suited for use in the next generation of European miniature atomic clock demonstrators.

Acknowledgment

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Bottom-Emitting VCSEL Arrays for Integrated Optical Particle Manipulation

Anna Bergmann

The purely optical manipulation of particles has gained increasing interest in recent years. Especially the combination of optical manipulation with microfluidics offers new possibilities, such as the contamination-free handling of micrometer-sized particles in biology and medicine without any mechanical contact. VCSELs (vertical-cavity surface-emitting lasers) are an excellent choice for optical trapping laser sources, offering the formation of two-dimensional arrays for parallel particle manipulation. Furthermore, they enable miniaturization by means of integration. In this report, we present a new concept for the realization of a so-called integrated optical trap. For this purpose, bottom-emitting AlGaAs–GaAs-based VCSEL arrays with a very small device pitch were fabricated and densely integrated with microfluidic channels.

1. Introduction

In 1970, Arthur Ashkin [1] reported the acceleration of particles by the radiation pressure of a laser beam, commonly called scattering force. Furthermore, he discovered an additional force which pulled the particles towards the laser beam center. Assuming a laser beam with a transverse (ideally Gaussian) intensity gradient, this effect can conveniently be explained by means of ray optics. All rays incident on a spherical particle are refracted and cause forces because of their change in momentum. The resulting net force points towards the maximum of intensity and is commonly called gradient force [2]. It increases with a stronger intensity gradient and is exploited in so-called optical traps which are useful tools for the manipulation of micrometer-sized particles. Optical manipulation offers the possibility of handling biological material without mechanical damage or contamination [3].

Microfluidic channels with widths and heights of typically several tens of micrometers enable the examination of biological samples with strongly reduced sample volumes, parallel cycling and exact timing [4, 5]. The combination of microfluidics and purely optical manipulation enables the non-mechanical handling of particles inside the channels [6, 7]. VCSELs are highly suitable for this field and have been investigated as trapping lasers in microfluidic channels [7–12]. One advantage of very common 850 nm VCSELs is their emission in the near-infrared range, where biological material has only little absorption. The vertical emission of VCSELs allows the fabrication of two-dimensional laser arrangements (arrays). Thus, patterns of multiple optical traps (or optical lattices) can be generated without the need for extensive beam splitting or steering setups. Besides the use of

VCSELs in a classical tweezers setup with objective lenses for beam collimation and focusing, even a strongly miniaturized setup can be realized by directly integrating VCSEL arrays and microfluidic channels. Thus, a portable, low-cost particle manipulation device is feasible, whereas one can hardly imagine the realization of similar integrated modules with other laser sources.

2. Bottom-Emitting VCSEL Arrays as Laser Sources for Optical Manipulation

VCSELs can be realized as top or bottom emitters. The schematic structure of a bottom-emitting VCSEL is depicted in Fig. 1. It is grown in the AlGaAs material system using molecular beam epitaxy, with a composition designed for an emission wavelength of around 850 nm. The laser resonator is built by distributed Bragg reflectors (DBRs). Top and bottom DBR are p- and n-doped, respectively, to achieve a p–i–n-like structure with an intrinsic active region. The bottom DBR has a reduced number of mirror pairs compared to the p-type DBR as this is the light outcoupling side of the VCSEL. The p-contacts are structured as full metal circles, in contrast to top-emitting VCSELs, where ring contacts are required. Such a full contact allows to reduce the mesa diameter and the device pitch in an array. The active region in the inner cavity consists of three 8 nm thick GaAs quantum wells, separated by 10 nm thick barriers. An AlGaAs layer with about 98 % aluminum content located above the active region is selectively oxidized after mesa etching, thus providing current confinement.

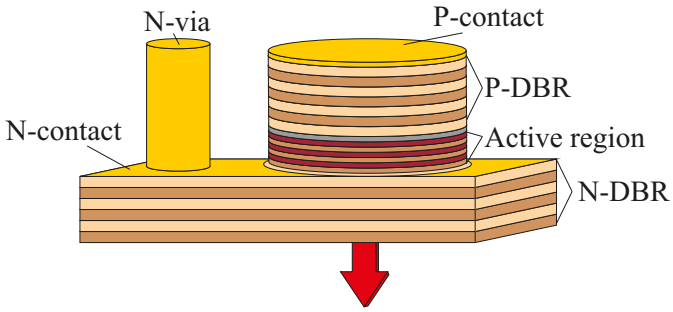

Fig. 1: Schematic of a bottom-emitting VCSEL structure with removed substrate and an n-via for flip-chip soldering.

Because VCSELs offer the advantageous possibility of creating various two-dimensional arrays, it is very obvious to realize patterns of optical traps, so-called optical lattices. They are based on the following principle [13, 14]: particles in liquid solution pass the optical trap array or optical lattice and are attracted to the beam centers of the individual lasers. If trapping force and fluidic drag force are in the same range, the particle can follow the lattice and is thus continuously deflected from its initial flow direction. By using two optical lattices and a microfluidic Y-junction, as indicated in Fig. 2, particles can be separated without mechanical or electrical intervention.

An ultra-dense spacing of the VCSELs is highly desirable for such optical lattices and a challenging requirement. The typical device pitch of commercial VCSELs for data

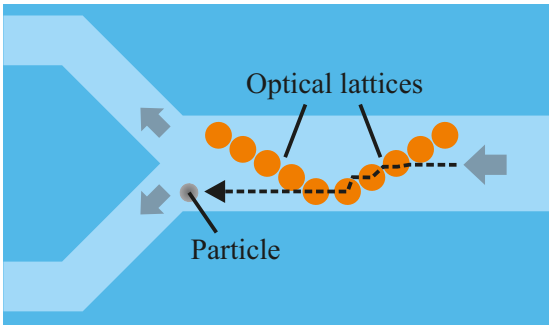

Fig. 2: Schematic particle separation by means of two optical lattices and a fluidic Y-junction.

communication applications is 250 µm [15]. For interruption-free optical manipulation this value needs to be reduced at least by an order of magnitude. Such a drastic reduction requires not only a minimized distance of about 2 µm between adjacent mesas but also reduced mesa diameters. As mentioned above, the full circle p-contact of bottom-emitting VCSELs helps to shrink the laser cross-section. The mesa diameters of the fabricated devices range from 16 to 20 µm, leading to device pitches from 18 to 22 µm.

3. Miniaturized Particle Deflection by an Integrated Optical Trap Concept

By means of tilted linear VCSEL arrays in a classical tweezers setup with objective lenses for beam forming, the continuous deflection of particles in aqueous solution was already demonstrated [16]. However, this setup is bulky and requires extensive alignment.

The so-called integrated optical trap represents a strongly miniaturized version of the classical tweezers setup where objective lenses are avoided. The trapping laser module with VCSEL arrays is directly integrated with the microfluidic chip. For an efficient particle deflection with the integrated optical lattice, the distance between microfluidic channel and trapping laser arrays must be minimized to reduce the beam expansion.

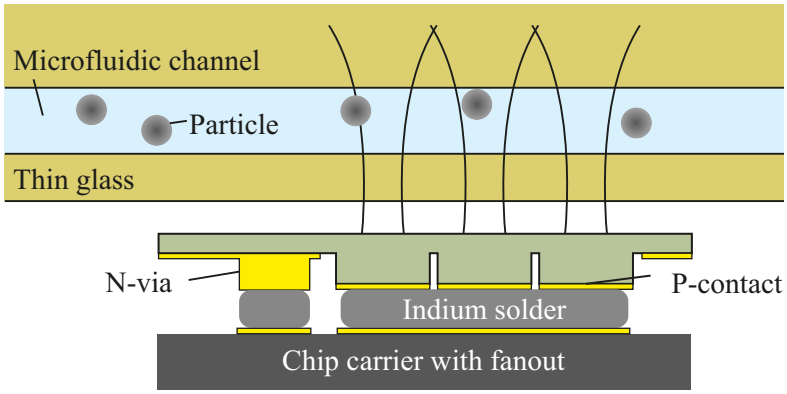

Fig. 3: Schematic of the novel integrated optical trap module. The bottom-emitting VCSEL chip is flip-chip soldered to a chip carrier and integrated with the microfluidic chip with a few micrometers distance.

Our integration approach for such an optical trap module is shown in Fig. 3. The flip-chip soldered laser chip with bottom-emitting VCSEL arrays is integrated with the microfluidic chip with a distance of only a few micrometers. Thus, the use of external optics can be avoided. By indium solder bumps, the laser chip is electrically connected to the chip carrier, where fanout tracks enable easy access to the electrical contacts after integration.

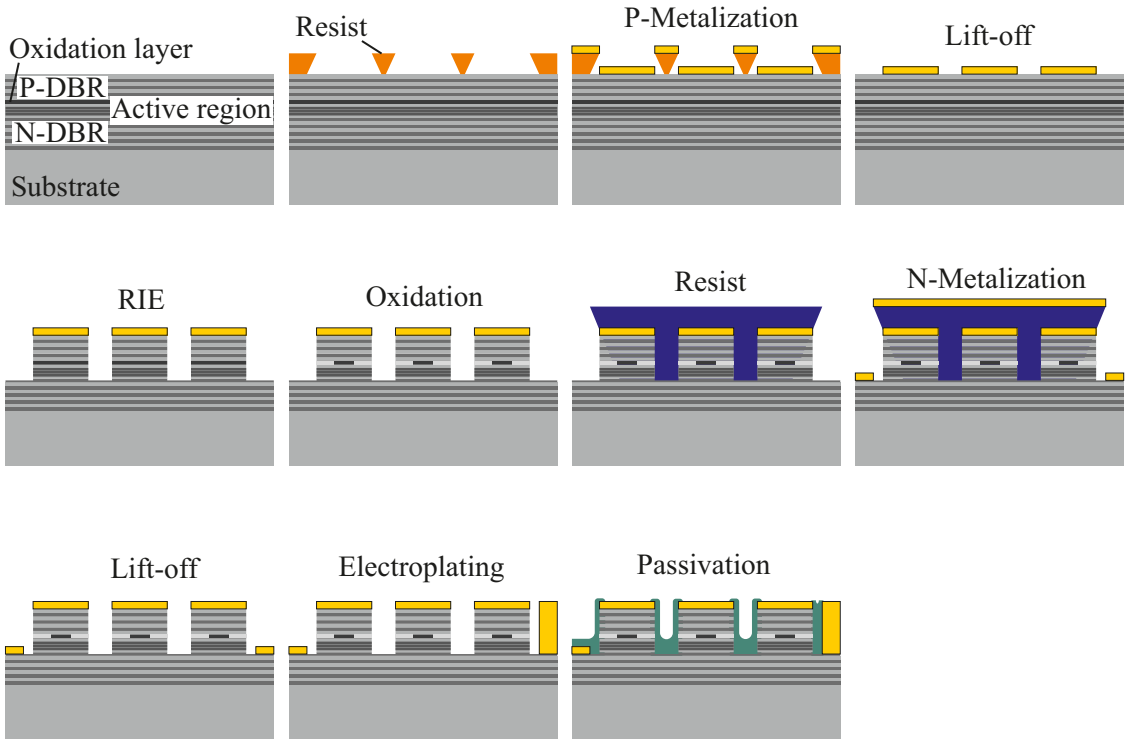

Fig. 4: Processing steps for the fabrication of densely packed bottom-emitting VCSEL arrays. Reactive-ion etching provides for vertical side walls needed for close spacing.

The processing steps for densely packed bottom-emitting VCSEL arrays are shown in Fig. 4. In the first step, the p-contacts are defined by photolithography, metal evaporation and lift-off. After that, the VCSEL mesas are defined by reactive-ion etching (RIE), where the metal of the p-contact serves as a stable etch mask. After etching, the oxidation layer is selectively oxidized by water vapor, with nitrogen as carrier gas. In the next step, the lasers are covered completely with photoresist and the etched region around the lasers is metalized. Close to the laser arrays, n-vias with the same height as the laser mesas are generated by electroplating. Thus, it is possible to solder the laser chips stably to the chip carriers. The fabrication of these carriers is shown in Fig. 5. Silicon with a high resistivity (ρ >15 kΩcm) and 380 µm thickness is covered with a 100 nm thick layer of Al_2O_3 to improve the electrical isolation. After that, fanout tracks are defined by lithography, metal evaporation and lift-off. The fanout metal is then electroplated to a thickness of approximately 2 µm. In the last step, indium bumps are structured to build the solder connection to the laser arrays and the n-vias on the laser chip.

Laser chip and carrier are combined by flip-chip soldering (Fig. 5), where the two components can be carefully aligned to each other. The melting indium creates both the electri-

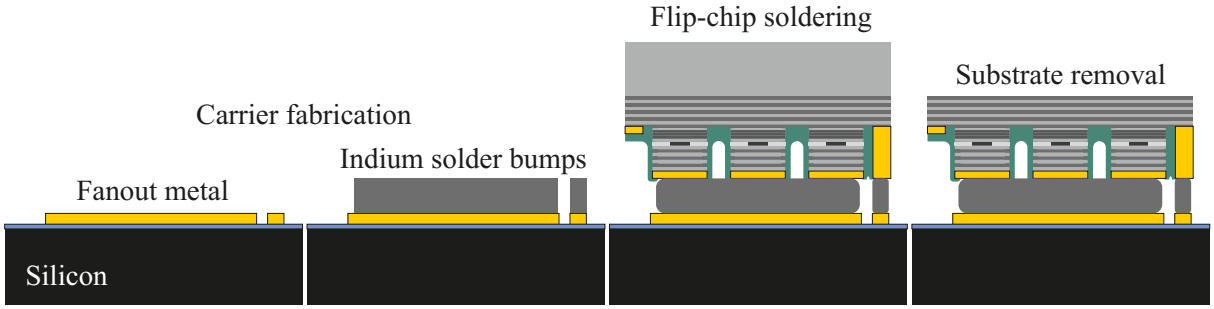

Fig. 5: Fabrication of silicon laser chip carriers with fanout tracks and indium solder bumps. By flip-chip soldering, laser chip and chip carrier are combined. Finally, the substrate on the back side of the laser chip is removed.

cal and mechanical connection. For a minimized distance between lasers and microfluidic channel, the substrate is wet-chemically removed. Thus, absorption of the 850 nm laser emission in the substrate is avoided as well. After substrate removal, the remaining structure is only a few micrometers thin. Figure 6 shows a microscope picture of an etched laser chip. The VCSEL arrays shine through the thin semiconductor material. At the corners of the laser chip, the n-vias are also visible.

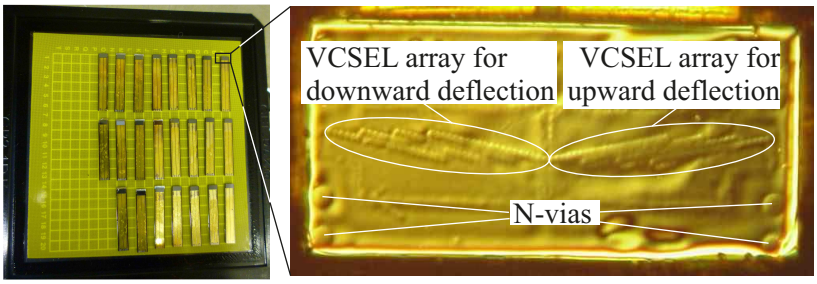

Fig. 6: Laser arrays at the tip of chip carriers in a sample box (left) and micrograph of a soldered laser chip with removed substrate (right). Both laser arrays and n-vias shine through the thin remaining semiconductor material.

The microfluidic channels are fabricated in polydimethylsiloxane (PDMS), a transparent and biocompatible polymer widely used for the manufacture of microfluidic chips [17]. In the first step, master wafers are fabricated which contain the inverse channel structures. A PDMS base (liquid) is mixed with a cross-linking agent and poured over the master wafer. The PDMS is then cured at 65°C and can be peeled off the reusable master wafer. Inlets from the top of the chip are created. By short exposure to an oxygen plasma, the channel can be sealed irreversibly with 30 µm thin glass.

For integration, laser arrays on the carrier and microfluidic channel are carefully aligned to each other. Observation during alignment is possible through the transparent microfluidic chip. For good adjustment, the laser chip can be moved in x-,y-, and z-directions, whereas the microfluidic chip can be rotated to adjust the tilt of the samples. After alignment, the components are fixed by an adhesive which is cured by ultraviolet light. A printed circuit board serves as the device platform and facilitates the handling.

4. Particle Experiments

The integrated VCSEL-based module described above was used for particle deflection. For this purpose, the microfluidic channel was filled with 15 µm polystyrene particles solved in water. Figure 7 shows snapshots of the experiment. The very left picture depicts the position of the lasers relative to the channel. Here, they were operated below threshold to make them visible. During the experiment, the laser power inside the channel was about 2.5 mW per laser with 25 lasers in total. Flow direction was from right to left. As the particle approached the lasers, it was attracted by the laser beams and at the same time pulled forward by the fluidic drag force. Thus, it was stepwise redirected from the channel center to the side wall of the 60 µm wide channel. Such deflection experiments have also been performed with other particle diameters to prove the flexible use of the device.

Fig. 7: Deflection experiment with a 15 µm polystyrene particle inside a microfluidic channel. The particle is stepwise redirected by the VCSELs in the array.

5. Conclusion

In this report we introduced bottom-emitting VCSEL arrays as excellent laser sources for combination with microfluidic channels. Owing to circular beam profiles, low power consumption, and arrangement in two-dimensional arrays, VCSELs are highly suitable for this purpose. By using VCSEL arrays as sources for optical trap patterns, continuous particle deflection becomes possible. We have shown our new approach for the integration of bottom-emitting VCSEL arrays with microfluidic channels, thus enabling miniaturized particle manipulation in compact, portable devices. We presented the fabrication of all necessary components as well as their integration. Finally, a particle manipulation experiment with an integrated particle deflection device was presented using 15 µm diameter polystyrene particles.

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MOVPE Growth of Semipolar GaN on Patterned Sapphire Wafers: Growth Optimisation and InGaN Quantum Wells

Tobias Meisch

We are able to achieve two different GaN semipolar surfaces by growing on patterned sapphire substrates: $(10\bar{1}1)$ *GaN on* $(11\bar{2}3)$ *sapphire and* $(11\bar{2}2)$ *on* $(10\bar{1}2)$*. By this approach, the growth of a coalesced semipolar layer on a large area of about two inches diameter is possible. Well known from the c-plane direction, an in-situ deposited SiN interlayer could reduce the defect density also in semipolar directions. The influence of position and growth temperature of the SiN layer on the GaN layer quality was investigated. Using optimized growth conditions, the full width at half maximum (FWHM) of X-ray rocking curve peaks could be halved. Moreover, an optimized temperature profile during growth of the main layer helps to improve the crystal quality even further. First InGaN quantum wells (QWs) were deposited on these optimized semipolar surfaces. When transferring the c-plane QW growth conditions to* $(11\bar{2}2)$ *GaN on* $(10\bar{1}2)$ *sapphire, a lower growth rate and a reduced indium incorporation was observed. By using thicker quantum wells grown with a higher indium flux, the emission wavelength could be shifted to 500 nm. In the case of* $(10\bar{1}1)$ *GaN on* $(11\bar{2}3)$ *sapphire, high-quality quantum wells with an emission wavelength of about 525 nm have been achieved.*

1. Introduction

Most of the common light emitting diodes or laser diodes based on InGaN/GaN are grown in the well-known c (0001) direction. On the one hand, excellent crystal quality can be obtained in such a direction, but on the other hand, the crystal symmetry of GaN causes strong piezoelectric fields within such heterostructures. These internal electric fields bend the energy levels leading to a charge carrier separation in the quantum wells. The reduced overlap of the wavefunctions of electrons and holes leads to a reduced recombination probability — the efficiency of a light emitting device decreases. In addition, a red-shifted emission wavelength as a result of a reduced effective bandgap is observable, known as quantum confined Stark effect (QCSE). To avoid or to reduce these internal electric fields, the growth in non-c-directions seems to be a promising way. However, growth in a non-polar direction is typically affected by a low crystal quality [1, 2]. Semipolar growth directions are a good compromise between an acceptable crystal quality and reduced QCSE.

One very interesting technique to grow GaN in the well-known c-direction obtaining yet a semipolar surface was presented for example by Okada et al. [3]: They patterned r-plane

sapphire substrates by etching trenches with c-like side facets into the wafer. With the help of selective epitaxy, crystal growth just on the c-facets is possible. At the beginning, GaN forms triangular shapes which eventually coalesce to a planar semipolar surface (cf. Fig. 1) after a suitable growth time.

Our investigations are focused on two different semipolar directions: $(10\bar{1}1)$ GaN on $(11\bar{2}3)$ patterned sapphire substrates and $(11\bar{2}2)$ GaN on $(10\bar{1}2)$ sapphire.

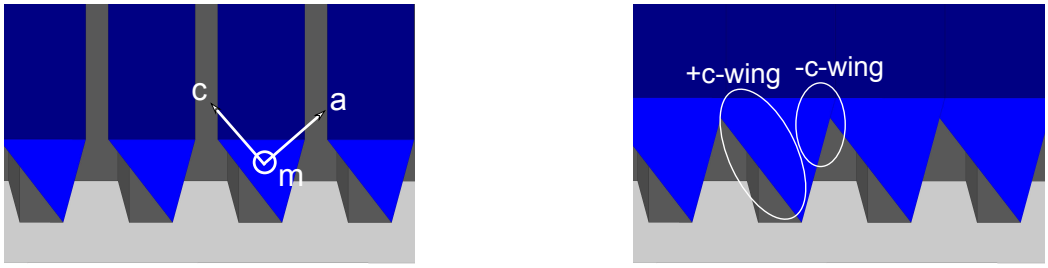

Fig. 1: Growth of GaN stripes (blue) with triangular shapes on a patterned substrate (grey). The triangular stripes (left) eventually coalesce to a planar surface (right).

2. Experimental

In order to pattern the sapphire substrate with trenches having a c-plane-like side facet, at first, a 200 nm thick layer of SiO_2 is deposited, which later acts as a mask for selective area growth. It is followed by an about 500 nm thick nickel layer structured via optical lithography with a stripe mask (3 µm opening, 6 µm period). The pattern is transferred into the sapphire by reactive ion etching. The resulting grooves have a width at the bottom of about 1.5 µm, a depth of about 1.2 µm and possess a c-plane-like facet.

All samples investigated in this study were grown in a low-pressure horizontal metal organic chemical vapor phase epitaxy (MOVPE) reactor with the precursors trimethylgallium (TMGa), trimethylaluminium (TMAl) and high purity ammonia. The growth starts with an oxygen-doped AlN nucleation layer at low temperature (about 960 °C), followed by a GaN buffer layer at about 1070 °C and a thick GaN top layer at 1030 °C. The reactor pressure was set to 150 mbar and the V/III ratio was 650. The crystal quality of the GaN layer was investigated by high resolution X-ray diffraction (HRXRD) and photoluminescence (PL) measurements. The surface morphology was mainly evaluated by scanning electron microscopy (SEM).

2.1 Growth optimisation

As already known from the growth of common c-plane GaN, an *in-situ* deposited thin SiN interlayer could reduce the defect density considerably (cf. Hertkorn et al. [4]). Similar as in an epitaxial lateral overgrowth procedure with an *ex-situ* deposited SiO_2 and lithographically structured mask, a great deal of the vertically running dislocations are stopped by the mask, and the remaining defects my be bent in a lateral direction. In the case of

our semipolar oriented GaN, the SiN interlayer is deposited after a thin high-temperature GaN buffer layer grown at about 1080 °C. Then, about 4 µm GaN are deposited at 1000 °C leading to full coalescence of the stripes. The corresponding photoluminescence spectra (cf. Fig. 2) for (11$\bar{2}$2) samples show a significant improvement of the crystal quality. By inserting the SiN nanomask layer, a doubling of the D^0X peak intensity at about 3.48 eV was achieved (cf. Fig. 2, left part), while the intensity of the stacking fault related signals at an energy of 3.42 eV decreased significantly (cf. Fig. 2, right part).

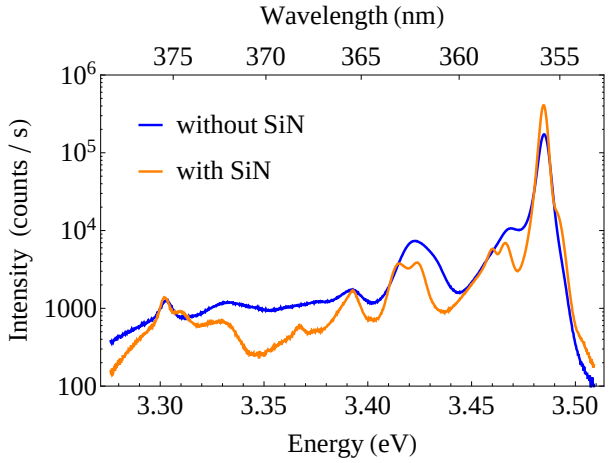

Fig. 2: Photoluminescence spectra of (11$\bar{2}$2) GaN with (orange) and without (blue) SiN interlayer. Introducing a SiN interlayer improves the crystal quality significantly, visible in a much higher D^0X intensity and a reduced intensity of the defect emission band (for example at 3.42 eV).

X-ray measurements of the symmetric (11$\bar{2}$2) and asymmetric (11$\bar{2}$4) reflections confirm the improvement of crystal quality (cf. Fig. 3). In particular, the FWHM of the asymmetric reflection decreases significantly.

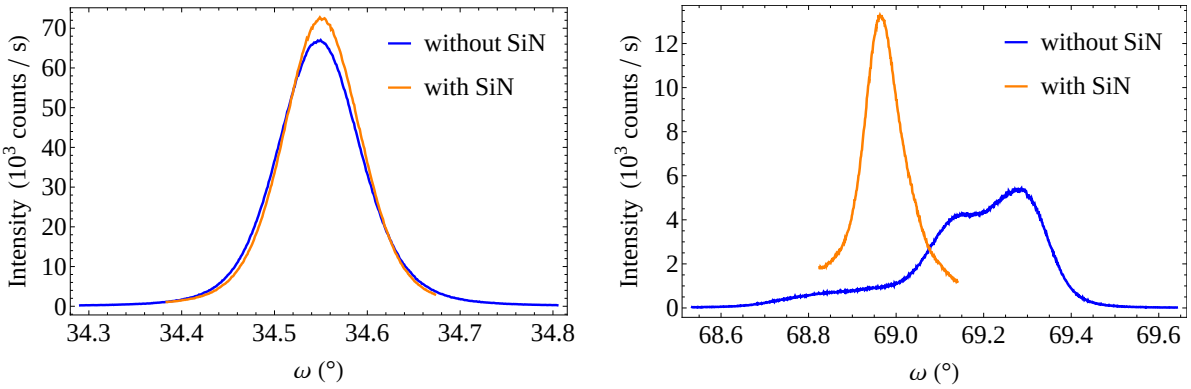

Fig. 3: Rocking curve (RC) measurements of (11$\bar{2}$2) GaN in (11$\bar{2}$2) (left) an (11$\bar{2}$4) (right) direction. The intensity of symmetric reflections (right) increases just slightly by inserting a SiN interlayer. However, asymmetric reflections (right) show a significant crystal quality improvement due to the SiN interlayer.

The influence of such a SiN interlayer on the growth of (10$\bar{1}$1) GaN was also investigated.

Using comparable growth conditions as for $(11\bar{2}2)$, the FWHM of the symmetric $(10\bar{1}1)$ X-ray reflection decreases from 770 arcsec to 510 arcsec. Although we have carefully studied further modifications of the growth conditions — like depositing temperature, thickness of buffer layer, etc. — we could not obtain a clear additional improvement. Previous cathodoluminescence (CL) investigations of Schwaiger et al. [5] showed that the −c-wing of our stripes (cf. Fig. 1) exhibits a higher defect density than the +c-wing. To take advantage of this given fact, an accelerated coalescence of the individual stripes could help to achieve a further crystal quality improvement. As shown in Fig. 4, for $(11\bar{2}2)$ layers, the +c-wing grows much faster than the −c-wing at first. By adding a cold top layer, the +c-wing coalesces with the left part of the adjacent +c-wing, whereas the growth of the −c-wing stops in a "dead end".

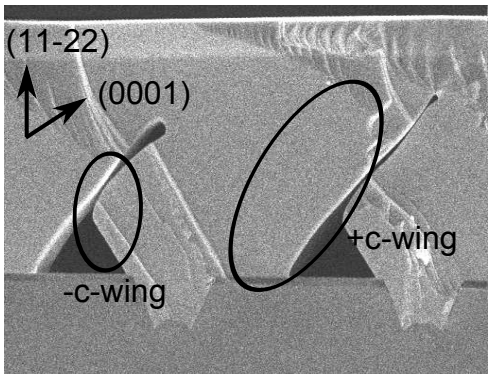

Fig. 4: Cross section SEM image of $(11\bar{2}2)$ GaN. Using slightly higher temperatures at the beginning of the growth, the stripes are not able to coalesce; a clear +c-wing and −c-wing, respectively, is visible. By adding a top layer, grown at reduced temperatures, the +c-wing gets pushed and overgrows the −c-wing, which exhibits an higher defect density. Due to the cold GaN top layer, the total defect density at the semipolar surface could be reduced significantly.

This effect may be pushed by growing a top layer at slightly reduced temperature. Therefore, we have grown three samples with different top layer temperatures. For temperatures of 1000 °C and 940 °C, we observe a reduced and broadened D^0X signal in PL (cf. Fig. 5), whereas a clear optimum is visible at a temperature of 970 °C. By this technique, the FWHM of the $(11\bar{2}2)$ rocking curves could be reduced to less than 200 arcsec. For the same growth direction, Okada et al. reported a FWHM of 211 arcsec [6].

2.2 Semipolar InGaN quantum wells

The improved quality of semipolar GaN with the help of a SiN interlayer and an additional cold top layer is now well-established and serves as a standard template recipe for subsequently deposited InGaN/GaN QW structures. By applying our standard quantum well growth conditions established for c-plane growth, five InGaN quantum wells at a temperature of about 775 °C were grown on a $(11\bar{2}2)$ template layer. The GaN barrier was deposited at a temperature of 835 °C. PL measurements show a significant difference to our c-plane reference sample grown in the same run: We measured a QW emission wavelength of 384 nm (cf. Fig. 6, left), whereas the (0001) QWs emit at 428 nm. By

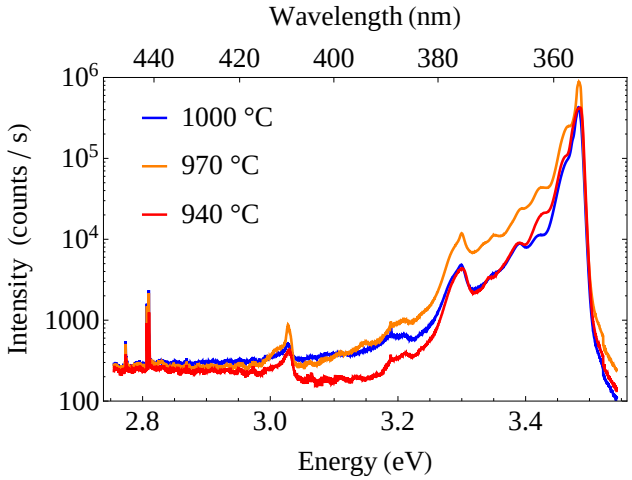

Fig. 5: Low-temperature PL spectra of $(11\bar{2}2)$ GaN with top layers grown at three different temperatures. For 970 °C, the GaN layer achieves an optimum crystal quality, indicated by the intensity of the D_0X emission at 3.482 eV.

evaluating the satellite peaks of HRXRD curves, we found indications for a significantly reduced QW periodicity in the case of the $(11\bar{2}2)$ sample (7.4 nm) compared to the c-plane counterpart (11.8 nm), translating into quantum well thicknesses of 2.5 and 4 nm, respectively. However, evaluations of the GaN growth rate at 1050 °C did not show such a difference (cf. Fig. 7). Hence, further investigations, e.g., TEM studies, should help to clarify this situation.

In the case of (0001) QWs, an emission wavelength of 428 nm is visible, whereas the $(11\bar{2}2)$ QWs emit at 384 nm (cf. Fig. 6, left). Measuring the quantum well dimensions via HRXRD shows a halved thickness in the case of $(11\bar{2}2)$ (2 nm) compared to c-plane (4 nm). Comparing the growth rate of (0001) and $(11\bar{2}2)$ GaN, it is conspicuous that they are exactly the same (cf. Fig. 7). TEM investigations should help to clarify this situation. However, in addition to the quantum well thickness, the piezoelectric field also plays an important role.

By doubling both, the indium flux and growth time of the $(11\bar{2}2)$ QWs, an emission wavelength of 424 nm was achieved (cf. Fig. 8, left), quite close to that of the c-plane reference sample. From the estimated InGaN layer thickness and the emission wavelength obtained on these samples, a rough estimation of their indium content is possible taking into account the different piezoelectric fields and quantization effects. In the case of the semipolar growth, an indium content of about 10 % is needed, to compensate the red-shift due to the QCSE in c-plane GaN (about 7 %). By increasing the indium flux from 53 µmol/min to 84 µmol/min, the emission wavelength could be further shifted to 486 nm, corresponding to an indium content of about 16 %. A sample with further increased quantum well thickness of about 6 nm emits at 500 nm. However, these green light emitting samples exhibit a strongly reduced quality, with just a weak signal of the quantum wells.

Similarly, quantum wells were grown on GaN. The InGaN layers were grown at a temperature of 735 °C and the GaN barriers at 800 °C. Using an indium flux of 42 µmol/min, a quantum well emission of 482 nm was achieved. By doubling the indium flux, the quantum

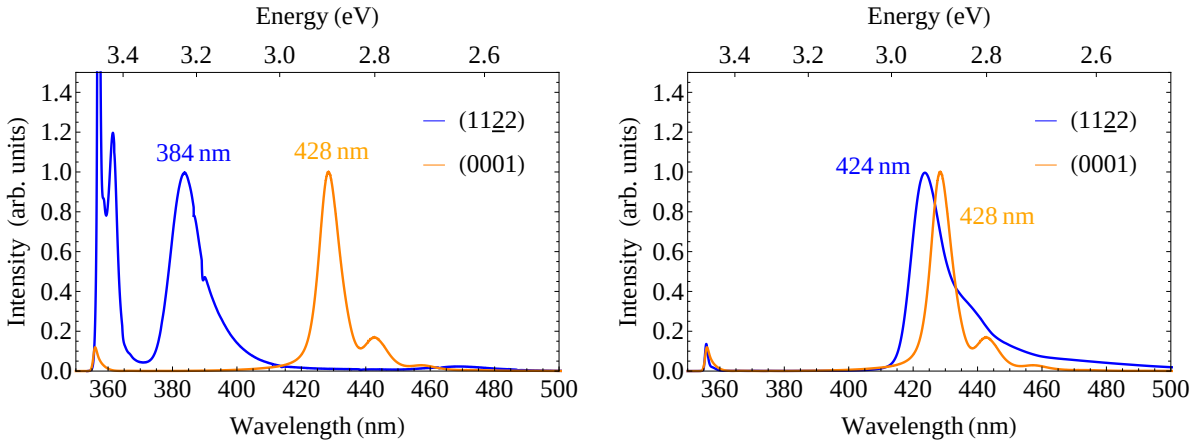

Fig. 6: Low-temperature PL measurements of (0001) (orange) and (11$\bar{2}$2) InGaN QWs (blue), respectively. When grown at comparable growth conditions, the semipolar QWs emit at shorter wavelength compared to the c-plane QWs (left). By doubling the growth time and the indium flux in the case of (11$\bar{2}$2) InGaN, the emission shifts from 384 nm to 424 nm (right).

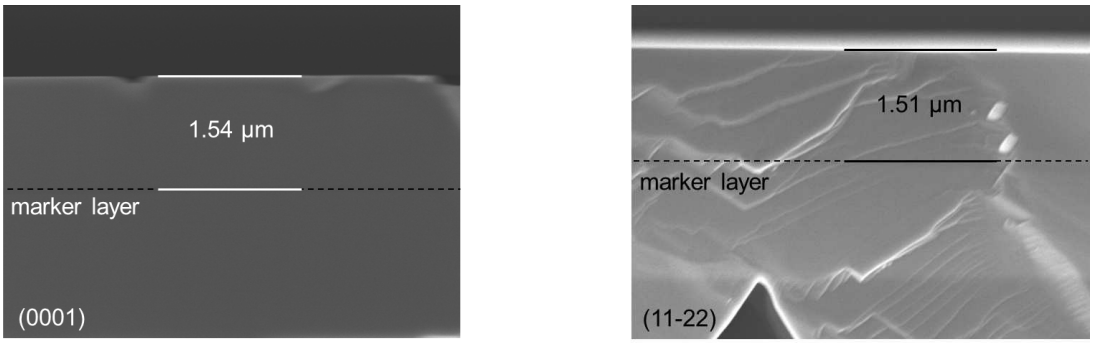

Fig. 7: Cross section SEM pictures of (0001) GaN (left) and (11$\bar{2}$2) GaN (right), respectively. Both samples were grown in one MOVPE run on different sapphire substrates. In both cases, we observed the same growth rate (within the limits of accuracy of the measurements).

well emission shifts into the green range to 525 nm. Obviously, the indium incorporation is significantly enhanced as compared to (11$\bar{2}$2), moreover, the quantum well quality on (10$\bar{1}$1) is much better, visible by a significantly higher PL intensity of the quantum wells. However, for the crystal quality of the pure GaN, we observed the opposite relation: the FWHM of the symmetric reflections of the (11$\bar{2}$2) rocking curves amount to less than 200 arcsec, whereas we found more than 400 arcsec for the respective (10$\bar{1}$1) sample.

A reduced quality of the (11$\bar{2}$2) InGaN quantum wells could be caused by a comparably rough surface morphology. We assume that an improved surface quality could help to improve the quantum well emission either. It turned out that the shape of the trench sidewalls has a big influence on the surface morphology. The sidewalls of the sapphire trenches, which were overgrown so far, has an angle of about 68 °(90 ° means perpendicular to the surface). However, the c-plane of the sapphire has an angle of 58 °. Changing the trench shape in such a way that the sidewall gets more c-plane-like shows very promising surface qualities.

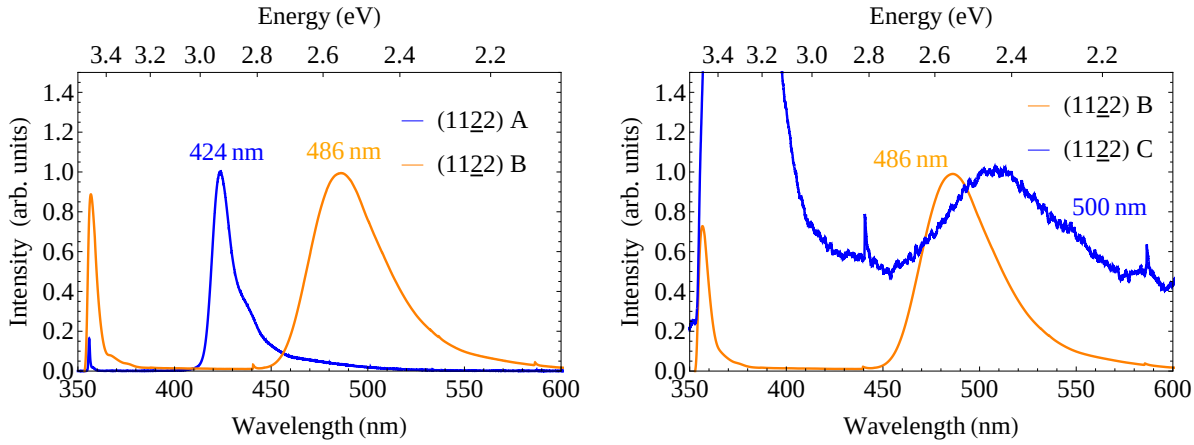

Fig. 8: Low temperature PL spectra of (11$\bar{2}$2) InGaN quantum wells, grown at various temperatures with different thicknesses. Sample A has a QW thickness of about 4 nm and was grown with an indium flux of 53 µmol/min. Increasing the indium flux to 84 µmol/min increases the QW emission wavelength to 486 nm (sample B). In the case of sample C, the quantum well thickness was increased to 6 nm.

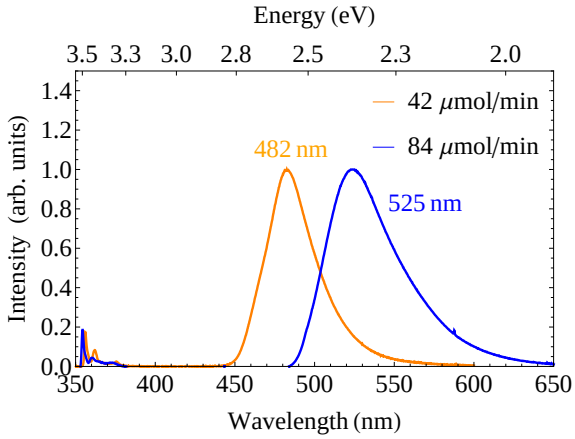

Fig. 9: Low temperature PL spectra of (10$\bar{1}$1) InGaN quantum wells with different indium flux.

3. Conclusion

By inserting a SiN interlayer in the epitaxial process of (11$\bar{2}$2) and (10$\bar{1}$1) GaN grown on structured sapphire wafers, we were able to improve the quality of large area semipolar GaN. An additional top layer of GaN, grown at slightly lower temperatures leads to a pronounced overgrowth of the +c-wing over the −c-wing, hence blocking the defects in this area. By these techniques, the total defect density could be reduced significantly. On such optimized semipolar GaN layers, we have deposited InGaN quantum wells. However, when pushing the In content to larger values, just a weak quantum well photoluminescence emission at longer wavelength is detectable for (11$\bar{2}$2) layers, whereas excellent properties have been measured on (10$\bar{1}$1) templates with a strong QW emission at 525 nm.

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Semipolar InGaN/GaN Converters for Bright Green Emission and Stripe Light Emitting Diodes

Junjun Wang

Optically pumped green converter structures based on three-dimensional (3D) inverse pyramids were studied. The green emission intensity is determined by the conversion rate η_c and the absorption fraction η_a, indicating the InGaN/GaN quantum well (QW) crystal quality and its absorption capability, respectively. 15 was found to be the optimal QW number based the epitaxial condition for that series of green converters while a smaller number decreases η_a and a larger number degrades the QW quality and then decreases η_c. The thermal budget was found to be a critical issue for the InGaN/GaN QWs with a high indium content. A low InGaN growth temperature is required to achieve green emission leading to an inferior InGaN quality. A larger thickness, a higher TMIn molar flow and a higher reactor pressure are helpful to increase the InGaN well growth temperature for a certain emission wavelength. However, the higher reactor pressure results in worse InGaN quality finally. Conventional light emitting diodes (LEDs) based on 3D stripes were also investigated. The leakage current is related to the local high density defects generated within the active region penetrating the p-GaN, probably at the apex. It was successfully suppressed by reducing the QW number from 5 to 1 and inserting an AlGaN layer in the p-side of the structures in some distance to the QWs.

1. Introduction

The droop problem is typically identified as an electroluminescence (EL) efficiency maximum obtained at comparably small current densities of about $10\,\mathrm{A/cm^2}$ in GaN-based LEDs and a continuously decreasing efficiency at higher current densities. Various reasons like Auger recombination [1] and electron spill-over [2] are controversially discussed. One solution is to decrease the carrier concentration in the QWs, which requires either wider or more QWs. While semipolar structures allow wider QWs compared to polar structures, an increase of the number of QWs in LED structures is difficult due to the strongly different injection efficiencies of electrons and holes from the n- and the p-side of the diode, respectively. This issue is aggravated for high In content QWs but can be circumvented by optical excitation of carriers leading to the idea of luminescence conversion structures with green light emitting InGaN QWs optically pumped with a highly efficient blue LED [3]. Thus, a more homogeneous excitation of a larger amount of QWs can be achieved. Moreover, electron spill-over can be avoided in such electrically un-biased converter structures. In this work, we optimized conversion structures with semipolar InGaN/GaN QWs based on our 3D structure approach for bright green emission. The crystal quality of the InGaN/GaN QWs is the most critical issue for the conversion structure. Hence, they were

grown based on the 3D structure of GaN inverse pyramids beneficial from its well optimized growth condition.

It is also interesting to investigate the conventional electrically-excited LEDs on our 3D structures since it saves the complicated processing procedure to integrate the conversion structures with excitation blue LEDs. For the 3D LEDs, the 3D profile of each layer, especially the undoped GaN spacer and the p-(Al)GaN layer, needs to well controlled in order to achieve nice electrical properties which are limiting factors in the current status. Thus, the 3D structure of stripes was applied in the LEDs to make the 3D profile control easier as explained in [4].

2. Semipolar InGaN Converters for Bright Green Emission

2.1 Characterization

In order to measure the efficiency of the luminescence conversion, the green converters were characterized by transmission experiments. The light beam of a 405 nm blue laser diode is coupled into the converter samples in most cases from the sapphire-side of the wafer (forward excitation). The outcoupled blue and green light is detected from the epi-side. The absorption fraction η_a (the intensity ratio between the absorbed and incoupled blue light) and the conversion rate η_c (the intensity ratio between the converted green and the absorbed blue light) can be determined. They are figures of merit for the QW absorption capability and the QW emission quality, respectively. The relation between the converted green and incoupled blue light can be expressed by

$$I_\mathrm{converted,g} = I_\mathrm{incoupled,b} \times \eta_\mathrm{a} \times \eta_\mathrm{c} \ . \tag{1}$$

A similar sample without any InGaN/GaN QWs was taken as a reference to compensate the light back-scattering at each interface along the light path since the light incoupling and outcoupling efficiencies are equal for the green converter and the reference sample. The absorption fraction η_a is calculated as

$$\eta_\mathrm{a} = \frac{I_\mathrm{outcoupled,b,r} - I_\mathrm{outcoupled,b}}{I_\mathrm{outcoupled,b,r}} \tag{2}$$

by evaluating the intensities of the outcoupled blue light for the green converter and the reference sample, indicated by $I_\mathrm{outcoupled,b}$ and $I_\mathrm{outcoupled,b,r}$, respectively. Assuming that the outcoupling efficiency η_e is equal for the blue and green light, the calculation of the conversion rate η_c can be expressed as

$$\eta_\mathrm{c} = \frac{I_\mathrm{converted,g} \times \eta_\mathrm{o}}{I_\mathrm{absorbed,b} \times \eta_\mathrm{o}} = \frac{I_\mathrm{outcoupled,g}}{I_\mathrm{outcoupled,b,r} - I_\mathrm{outcoupled,b}} \ . \tag{3}$$

The overall intensity of the outcoupled light in front of the sample is achieved by integrating the light intensity over the semispheric surface. As shown in Fig. 1, the outcoupled blue light is distributed center-symmetrically with a six-fold pattern as a consequence of our hexagonal pyramidal surface structure. Hence, the mapping of the area normalized

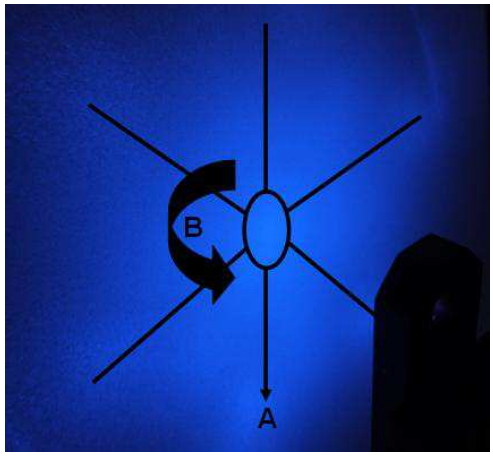

Fig. 1: The outcoupled blue light intensity distribution of the reference sample on a screen. The six straight lines show the six-fold pattern with the center indicated by the ellipse. Two dimensional angle-resolved measurements are performed along the radial (A) and circular (B) directions.

light intensity is performed via angle-resolved measurements in the radial direction indicated as A and the circular direction indicated by the rotation angle B in Fig. 1. The case of the outcoupled green light is even simpler since its distribution is center-symmetrical and constant along the circular direction.

The absorption coefficient α can be calculated from the absorption fraction η_a by

$$1 - \eta_\mathrm{a} = e^{-2\alpha n d} \tag{4}$$

where n and d represent the number and the thickness of the QWs, respectively. Since our semipolar QWs are tilted by 60 ° with respect to the substrate surface, the path of the blue light through the QWs is actually twice of the QW thickness which gives the factor of 2 in 4. With the same QW number, the doubled light path in our tilted QWs compared to the planar ones results in a strong absorption of the blue light in our structures.

2.2 Results and discussion

As mentioned above, the possibility to increase the number of QWs is a significant advantage of such optically pumped structures, which increases the overall absorption of the excitation light and hence potentially the green light intensity. However, two things must be considered when doing so: On one hand, late grown QWs may have lower quality as they are grown on already strained sub-layers. On the other hand, early grown QWs are longer subjected to high temperatures which may degrade their quality. Hence, an optimum has to be found concerning the number of QWs. To this end, we have grown three samples (samples 1, 2 and 3) with 10, 15 and 20 QWs, respectively, all emitting at the same wavelength of 505 nm. Indeed, the absorption fraction η_a rises with increasing QW number as expected, exceeding 90 % for the samples with 15 and 20 QWs. Although the electron and hole distributions are much more homogeneous for optically pumped green

converters compared to electrical pumping in conventional LEDs, the amount of electrons and holes within the QWs decreases exponentially with respect to the penetration depth of the blue pump light. Thus, the overall performance will depend more strongly on the quality of the QWs closer to the excitation source. Samples 1 and 2, with 10 and 15 QWs, respectively, have similar values for η_c, 4.9 % and 5.1 %, indicating comparable QW quality and the higher number of QWs results in a brighter total green emission. However, for sample 3 the further addition of 5 QWs leads to a reduction of η_c by 0.9 % compared to sample 2 indicating an inferior crystalline quality for the higher number of QWs which counters and outweighs the higher absorption of blue light. As explained above, this may be caused by not only the larger thermal load experienced by early grown QWs during the longer overgrowth but also the more defective late grown QWs. With the epitaxy conditions for this series of samples, sample 2 has the strongest green emission achieving a balance between the parameters η_a and η_c.

Table 1: Result of the transmission experiment for samples 1–5 with forward excitation ($\lambda = 505\,\mathrm{nm}$).

Sample no.	1	2	3	4	5
QW number	10	15	20	2×5	4×5
η_a	85 %	92 %	95 %	87 %	93 %
α ($10^5\,\mathrm{cm}^{-1}$)	3.8	3.4	2.9	4.0	2.6
η_c	4.9 %	5.1 %	4.2 %	2.6 %	2.6 %

In order to reduce strain related defects and to improve the quality of the late grown QWs, groups of 5 QWs each were separated by inserting about 50 nm GaN, thus reducing the average In content of the active layer. Two samples with 2×5 QWs and 4×5 QWs (samples 4 and 5 in Table 1) were produced. While the samples with the same number of QWs (samples 1 and 4; samples 3 and 5) have similar values of η_a, the samples with separated groups of QWs have substantially decreased values for η_c. This is attributed to the extra thermal load caused by the growth of the GaN layer between each two groups of 5 QWs which seems to be more important than the reduced strain.

All of the 5 samples (samples 1–5) have similar values for the absorption coefficient α which confirms comparable absorption capability for the InGaN material with the same indium content.

As discussed above, the absorption in the QWs farther from the excitation source is much weaker than that in the ones close to it. Hence, the QWs with better quality should be placed closer to the excitation source to enhance the green emission intensity. When the green converter is placed with its epi-side facing the 405 nm laser, most of the pump light is absorbed in the topmost QWs and the measured light leaves the sample from the sapphire-side. We refer to such an experimental setup as backward excitation while the previously mentioned transmission experiment is named forward excitation. As seen in Table 2, η_a is pretty similar for the forward and backward excitation, respectively, for all

5 samples. Interestingly, η_c is enhanced by nearly 90 % in backward excitation for sample 3. This result shows that the late grown QWs which are not subjected to a large thermal load have a better quality than the early grown ones and further optimization for samples with high numbers of QWs should specifically address the issue of thermal budget.

Table 2: Result of the transmission experiment for samples 1–5 with backward excitation ($\lambda = 505\,\mathrm{nm}$).

Sample no.	1	2	3	4	5
QW number	10	15	20	2×5	4×5
η_a	89 %	91 %	94 %	89 %	95 %
α ($10^5\,\mathrm{cm}^{-1}$)	4.4	3.2	2.7	4.4	3.1
η_c	8.6 %	8.2 %	7.9 %	3.7 %	3.2 %

For a long emission wavelength above 500 nm, a low growth temperature below 800 °C is required for the InGaN wells leading to a degraded material quality. We tried to improve the InGaN material quality by increasing its growth temperature while a larger InGaN well thickness, a higher TMIn (trimethylindium) flow rate and a higher reactor pressure are applied to compensate the emission wavelength blueshift. For this purpose, green converters with 5 InGaN/GaN QWs were fabricated under different InGaN growth conditions.

Table 3: Result of the transmission experiment for samples 6–8 with forward excitation ($\lambda = 510\,\mathrm{nm}$).

Sample no.	6	7	8
nominal QW thickness (nm)	2.5	3.5	5.0
InGaN growth T (°C)	710	714	721
η_a	51 %	65 %	72 %
α ($10^5\,\mathrm{cm}^{-1}$)	2.9	3.0	2.5
η_c	6.9 %	6.9 %	7.7 %

As listed in Table 3, three samples (samples 6, 7 and 8) were prepared with a nominal InGaN well thickness of 2.5 nm, 3.5 nm and 5.0 nm, respectively. η_a rises with increasing nominal InGaN well thickness, in other words, with increasing effective total InGaN thickness while the intrinsic property of the InGaN material α is quite similar among these three samples. The required InGaN growth temperature is higher for thicker QWs to obtain a certain emission wavelength. In the case of c-plane InGaN/GaN QWs, the luminescence efficiency drops with increasing QW thickness caused by the quantum-confined Stark effect outweighing the benefit from the higher InGaN growth temperature. Owing to the reduced piezoelectric field, this negative effect is not as strong in our semipolar

InGaN/GaN QWs as that on the c-plane ones. η_c is 6.9 % for both of samples 6 and 7 and increases to 7.7 % for sample 8. So a larger QW thickness is helpful to enhance η_a and η_c at the same time.

Table 4: Result of the transmission experiment for samples 9–11 with backward excitation ($\lambda = 518\,\mathrm{nm}$).

Sample no.	9	10	11
TMIn molar flow rate (µmole/min)	26.4	39.8	53.0
InGaN growth T (°C)	755	782	790
η_a	90 %	87 %	88 %
α ($10^5\,\mathrm{cm}^{-1}$)	4.6	4.0	4.2
η_c	5.5 %	10.3 %	7.8 %

As listed in Table 4, three samples (samples 9, 10 and 11) were prepared with a TMIn molar flow rate of 26 µmole/min, 40 µmole/min and 53 µmole/min, respectively. The required InGaN growth temperature to achieve the emission wavelength of 518 nm is enhanced by about 17 °C when the TMIn molar flow rate increases from 26 µmole/min to 40 µmole/min leading to almost a doubled value of η_c. However, further enhancement of TMIn molar flow reduces η_c probably due to changes in microscopic InGaN growth mechanism.

Table 5: Result of the transmission experiment for samples 12 and 13 with backward excitation ($\lambda = 510\,\mathrm{nm}$).

Sample no.	12	13
reactor pressure (hPa)	200	400
InGaN growth T (°C)	758	765
η_a	83 %	85 %
α ($10^5\,\mathrm{cm}^{-1}$)	3.5	3.8
η_c	12.0 %	6.9 %

As listed in Table 5, two samples (samples 12 and 13) were prepared with reactor pressures of 200 hPa and 400 hPa, respectively. A high reactor pressure can indeed increase the required InGaN growth temperature for the emission wavelength of 510 nm, but results in a smaller η_c indicating an inferior InGaN crystal quality.

3. Stripe Light Emitting Diodes

In this section, we investigate conventional electrically pumped LEDs with semipolar InGaN/GaN QWs on the side facets of periodic stripes.

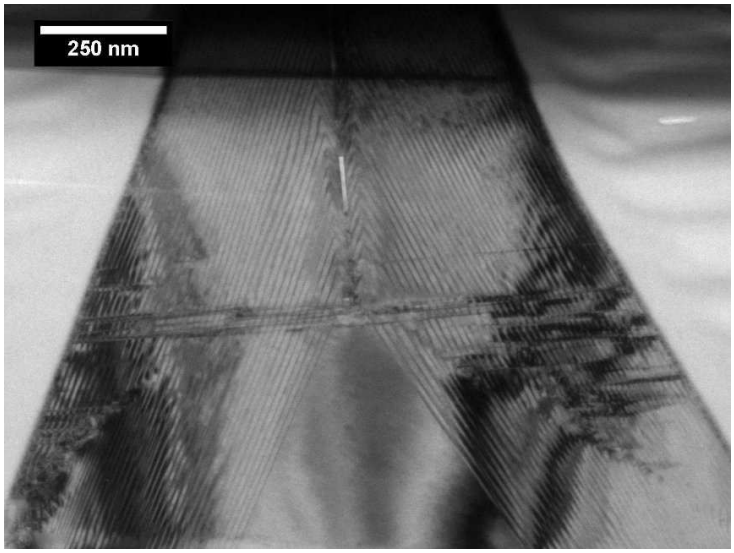

Fig. 2: Cross-sectional TEM image of a converter structure with 40 InGaN/GaN QWs.

The stripe LED with 5 InGaN/GaN QWs generates an output power of 340 µW at 58 mA and breaks down afterwards with increasing current. The leakage current at a reverse bias of 5 V is as high as ∼3 mA. A high density of defects through the diode may be responsible for the big leakage current. A cross-sectional TEM (transmission electron microscope) image of a converter structure with 40 InGaN/GaN QWs shows a high defect density within the active region at the stripe apex and stacking fault arrays originated at the stripe apex running horizontally (Fig. 2). It was reported that AlN layers can terminate such stacking faults [5]. Hence, we aimed to block the leakage current by including an AlGaN layer within our stripe LED structure either directly above the undoped GaN spacer or above ∼50 nm Mg:GaN (Fig. 3). In the former case, the AlGaN layer performs simultaneously as electron blocking layer (EBL). In the latter case, the tip is better

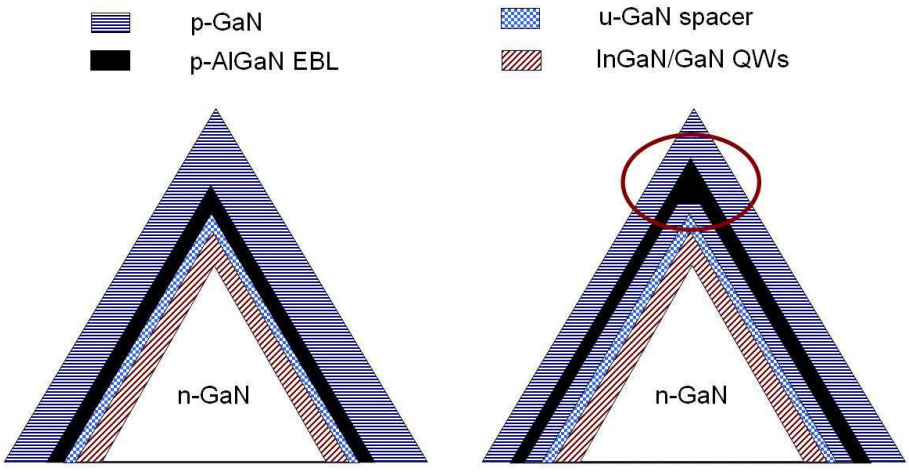

Fig. 3: Schematic structures for the stripe LEDs with an AlGaN layer directly on undoped GaN spacer (left) and above ∼50 nm Mg:GaN (right).

blocked by a thicker AlGaN layer there: Mg doing induces lateral growth [6] resulting in a plateau on the c-plane surface after ∼50 nm Mg:GaN growth. The following AlGaN layer grows more vertically, rebuilding the sharp tip and leading to a larger thickness there. The leakage current stays in the same order or even gets higher with the addition of the AlGaN EBL while it is successfully reduced from ∼3 mA to ∼0.3 mA by inserting the up-shifted AlGaN layer (Table 6). With the heavily reduced leakage current, the LED with the up-shifted AlGaN layer shows quite promising performance in EL. It works stably up to ∼120 mA without the diode breakdown indicating suppressed local current crowding, especially at the tip (Fig. 4). However, the LED with the up-shifted AlGaN layer still has a lower output power than the one without any AlGAN layer, probably due to a reduced hole injection. So further optimization is required for the Al-content, thickness and position of the up-shifted AlGaN layer.

Table 6: Leakage currents at −5 V for LEDs with 5 QWs (without any AlGaN layer, with the AlGaN EBL and the up-shifted AlGaN layer) and with a single QW.

	no AlGaN	AlGaN EBL	up-shifted AlGaN	no AlGaN
QW number	5	5	5	1
Leakage current at −5 V	3 mA	5 mA	0.3 mA	1 mA

A single-QW LED should have a smaller defect density within the active region compared to a 5QW one due to the reduced strain. This may lead to a lower leakage current. One single-QW LED was produced without any AlGaN layer which may affect the hole injection negatively. Indeed, this sample has a smaller leakage current of ∼1 mA compared to the 5QW LED as expected (Table 6). This LED also gives a quite high output power of 0.53 mW at 70 mA in EL (Fig. 4).

As discussed, conventional Mg doping induces lateral growth resulting in a plateau on the Mg:GaN surface with the sharp Si:GaN apex underneath. When the contact metal gets direct contact to the QWs, short circuits can occur. To overcome this problem, the technique of 'pulse doping' (the metalorganics and NH_3 are supplied alternatively in pulses) was applied for all the stripe LEDs mentioned above to push the Mg:GaN growth vertically [6]. The Mg:GaN was grown with conventional doping for the bottom and top layers, but with pulse doping in the middle layer. The up-shifted AlGaN layer was placed on top of conventionally-doped Mg:GaN. However, the Mg:GaN growth rate with the pulse doping technique is only about 1/3 of that of the conventional Mg:GaN. The thermal load is very critical for the green InGaN/GaN QWs degrading the InGaN crystal quality heavily via indium segregation [7]. The required longer growth time of the pulse-doped p-GaN aggravates the thermal load for the underlying InGaN/GaN QWs. Therefore, we have developed a procedure called 'triple p-GaN' which can push the vertical Mg:GaN growth without decreasing the growth rate. It starts with a high Mg doping level in order to achieve sufficient p-conductivity during which a c-plane plateau is developed. Then, a thin Mg:GaN layer with a low Mg doping level rebuilds the sharp apex, preventing any direct contact between the QWs and the metal contact. The third Mg:GaN layer is

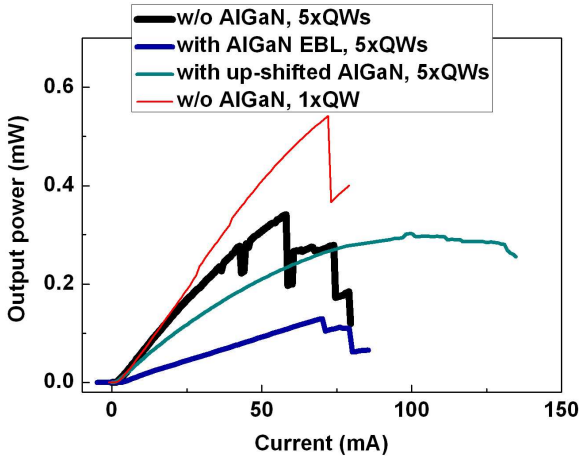

Fig. 4: EL output power against current for all the samples in Table 6.

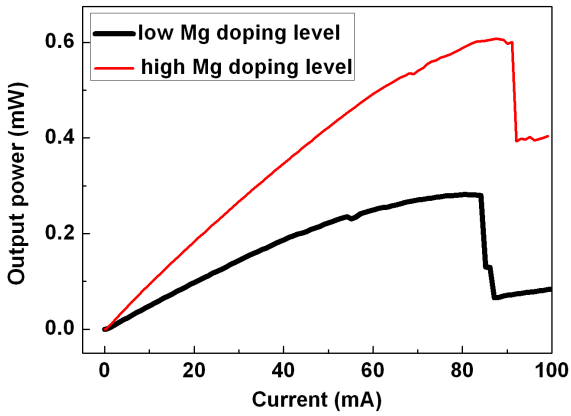

Fig. 5: EL output power against current for 5QW stripe LEDs with the up-shifted AlGaN layer and the triple p-GaN layer, one with a higher Mg doping level in the middle p-GaN layer compared to the other.

highly doped to obtain good contact properties. Two 5QW stripe LEDs were prepared with the up-shifted AlGaN layer and the triple p-GaN. The Mg doping level is increased for the second LED in the middle slightly-doped p-GaN layer. Strongly reduced leakage currents of ∼30 µA and ∼15 µA, respectively, have been obtained. In order to completely understand these promising results, more investigations, for example TEM and µ-EL, are currently underway. As seen in Fig. 5, the enhanced Mg doping level in the middle slightly-doped p-GaN layer doubled the output power in EL due to improved hole injection. The LED with higher Mg doping level in the middle p-GaN layer gives an output power of 0.54 mW at 70 mA and works stably up to 90 mA.

4. Conclusion

In order to optimize luminescence conversion structures with semipolar QWs for the generation of green light, we varied several parameters of our QW structures. We found an optimal QW number of 15 based on the epitaxy conditions for that series of samples with different QW numbers. Obviously, a much smaller number of semipolar InGaN/GaN QWs is necessary to achieve sufficient blue light absorption compared to c-plane ones [3]. The thermal budget is a very critical issue for the InGaN crystal quality. A high InGaN growth temperature is beneficial for the InGaN crystal quality. In order to enable a higher growth temperature of the QWs, we studied structures with thicker QWs, a higher TMIn molar flow rate and a higher reactor pressure aiming at the same emission wavelength. Both, absorption fraction η_a and conversion rate η_c increase with thicker QWs. With an increased TMIn molar flow rate, $\eta_c = 10.3\,\%$ was realized at the emission wavelength of 518 nm with $\eta_a = 87\,\%$. A higher reactor pressure can help increase In uptake and hence to increase the InGaN growth temperature but eventually results in an inferior InGaN crystal quality.

In electrically driven semipolar LED structures, we observed that the leakage current is smaller in single-QW stripe LEDs than in 5QW ones due to the reduced defect density, especially at the stripe apex. We successfully decreased the leakage current by incorporating an AlGaN layer in the p-side of the structures in some distance to the QWs. In order to improve the shape of the GaN:Mg layer near the apex of our stripes, we applied special techniques like pulse doped p-GaN and triple p-GaN to push the Mg:GaN growth vertically. The growth rate of the triple p-GaN is 3 times of that of the pulse doped p-GaN thus reducing the thermal budget for the underlying InGaN/GaN QWs. A higher Mg doping level in the middle p-GaN layer of the triple p-GaN doubled the output power in EL due to improved hole injection.

Acknowledgment

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Optimization of GaN Based Light Emitters With Semipolar Quantum Wells and Sub-μm Patterning Within the Active Zone

Robert A. R. Leute

The selective growth of sub-micrometer sized GaN stripes running along a-direction on c-oriented GaN templates results in semipolar quantum wells (QWs) grown on the $\{10\bar{1}1\}$ *side facets that can be embedded easily. Therefore we achieve light emitting devices with semipolar quantum wells on large areas with flat surfaces for easy processing. The influence of the growth mask is thoroughly investigated and structural analysis of the embedded QWs is presented.*

1. Introduction

There is a high scientific interest in semipolar GaN crystal planes for efficient long wavelength light emitters [1, 2]. The use of free-standing GaN templates for homoepitaxy is favoured by many groups [3–5]. However, the high cost and small size of commercially available semipolar GaN substrates motivates the pursuit of heteroepitaxial alternatives [6]. Three-dimensional GaN structures, based on growth in c-direction, with semipolar side facets are especially attractive, since they can be grown on large and inexpensive foreign substrates with high crystal quality [7]. For device processing, however, planar surfaces are favored, allowing conventional structuring methods for contacts, resonator formation, etc. This can be achieved by reducing the size of the 3D GaN to a few hundred nanometers and embedding the active, semipolar QWs within c-plane layers. Over the course of the year 2011 a patterning process based on laser interference lithography was established within the Institute of Optoelectronics [8] and first light emitting diodes (LEDs) with embedded GaN stripes were presented. In the following, we present the optimization of the processing. The influence of the growth mask is investigated and structural analysis of the embedded quantum wells by transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) is shown. This was partly published in [9].

2. Experimental

All epitaxial growth is done in an Aixtron-200/4RF-S HT MOVPE reactor with standard precursors. Silane and Cp_2Mg are used for doping; Pd diffused hydrogen and high purity nitrogen are used as carrier gases. About 3 μm thick c-oriented GaN templates are grown on c-plane sapphire with conventional growth conditions. We use an oxygen doped AlN

nucleation layer as well as an in-situ SiN interlayer to reduce the defect density [10]. The topmost layer of 1.8 µm thickness is silicon-doped to achieve a nominal doping level of $3.5 \times 10^{18}\,\mathrm{cm}^{-3}$.

For laser interference lithography, the beam of a HeCd laser ($\lambda = 325\,\mathrm{nm}$) is expanded by a lens and spatially filtered with a pinhole. Half of the beam hits the sample directly, the other half is reflected by a mirror, positioned very close to the sample with an angle of about 90°. Both beam halves interfere with each other and create a stripe pattern with a periodicity as low as 230 nm on an area of a semicircle with a diameter of 2.5 cm to 3 cm. The geometry is based on Lloyd's mirror [11]. The alignment of sample and mirror was chosen to result in resist stripes running parallel to the *a*-axis in GaN. A thin layer (15 nm) of titanium is subsequently deposited onto the structured templates by electron-beam evaporation and the pattern is transferred via lift-off. The templates are then cleaned with an aqueous KOH solution and re-loaded into the MOVPE reactor where the Ti mask is nitridized *in-situ*. Afterwards, the second growth step is carried out, consisting of n-doped stripes with $\{10\bar{1}1\}$ side facets, two InGaN quantum wells, an undoped spacer and finally a p-doped planarization layer. The epitaxial structure includes neither an electron blocking layer nor an InGaN pre-well common to c-plane LEDs. The stripes are grown for 120 s at 950°C with a V/III ratio of 260. The QWs are grown at 760°C with TEGa and nitrogen as carrier gas for 460 nm emission wavelength. The spacer is grown first at 950°C, then temperature is increased to 1000°C. For the embedding p-GaN layer the temperature was varied from 1000°C to 1090°C while the V/III ratio was kept at 1080.

For electrical characterization, the LEDs were annealed in an ambient atmosphere at 750°C for 60 s to activate the Mg-acceptors, then 1 µm thick circular indium contacts were evaporated onto the p-side of the LED.

2.1 Optical characerization and influence of mask material

The devices exhibit a highly polarized light emission (shown in Fig. 1) due to the semipolar character of the quantum wells and the regular arrangement of the stripes [12], however the intensity is rather low.

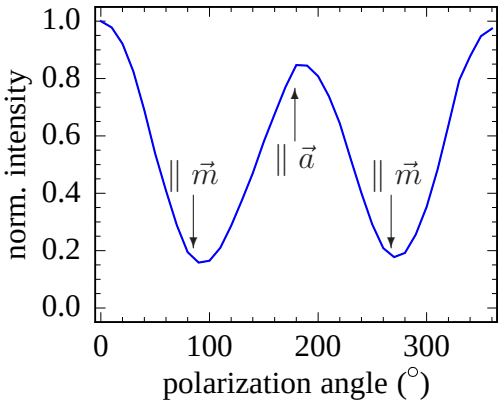

Fig. 1: Polarization dependent measurement of the emission from the semipolar QWs. Polarization angle is given relative to the orientation of stripes.

Transmission electron microscopy (TEM) measurements were performed by J. Thalmair at the University of Regensburg in the group of Prof. J. Zweck to investigate the reasons for the low light output. Figure 2 shows a TEM picture of the embedded active zone with well-developed QWs of 3 nm thickness. Figure 3 however reveals that in some areas c-plane surfaces exist with QWs which are over 10 nm thick, which would result in a nominal emission wavelength as long as 800 nm if we assume an identical indium content. Nonradiative recombination dominates in these thick c-plane QWs due to the intrinsic piezoelectric field and hamper the performance of the LED.

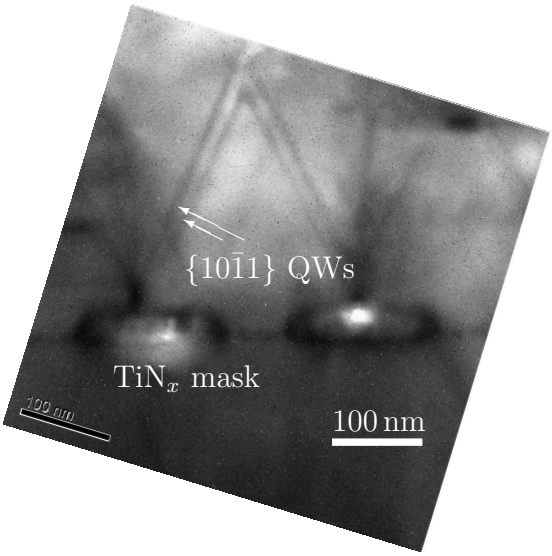

Fig. 2: TEM cross section of the embedded active region with well developed semipolar quantum wells.

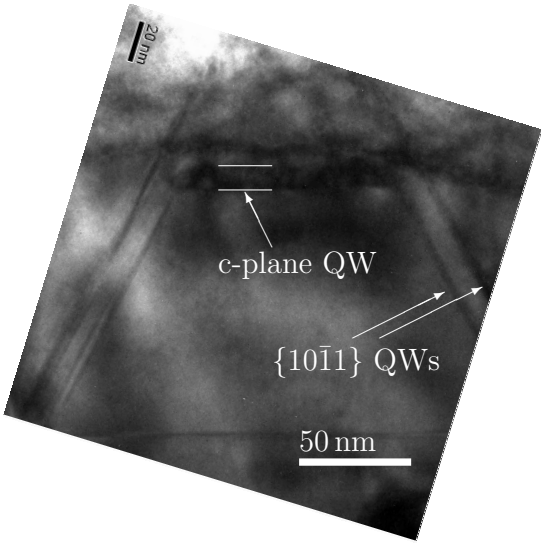

Fig. 3: TEM cross section view of a region where adjacent stripes coalesced and formed a c-plane surface. The c-plane QW is enlarged.

In order to exclude the influence of c-plane QWs, reference samples were structured by electron-beam lithography with a honeycomb pattern. The resulting sub-micrometer sized inverse pyramids have {10$\bar{1}$1} side facets, too, and show almost no c-plane surfaces at all within the patterned area. All growth parameters were kept identical to the stripe samples. A planarized LED with such structures within the active region showed an improved output power, see Fig. 4, corroborating the negative effect of the c-plane areas.

The immediate vicinity of the TiN_x mask to the active zone of the LEDs further influences the device performance. We assume that TiN_x absorbs substantial fractions of the light created within the active region of the LED as well as increases leakage currents due to its metallic character. Ex-situ removal of the TiN_x mask after the growth of the 3D GaN stripes with a mixture of hydrogen peroxide and sulfuric acid resulted in a tenfold increase of the output power and a decrase of the leakage current at reverse bias, compared to a similar sample where the TiN mask remained embedded. Therefore, efforts were undertaken to replace the TiN_x mask by a dielectric SiO_2 or SiN_x mask. Patterning via lift-off of sputtered SiO_2 proved impractical and was replaced by pattern transfer through dry etching with a fluorine containing plasma.

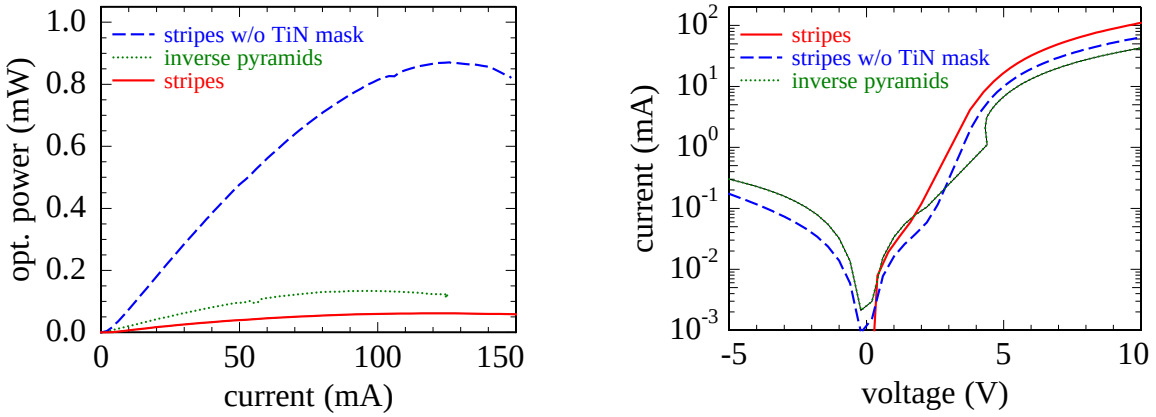

Fig. 4: Power–current (left) and current–voltage (right) characteristics for semipolar LEDs with embedded 3D structures. A substantial increase of power was achieved by embedding inverse pyramids. A huge increase was achieved by ex-situ removal of the TiN_x mask.

2.2 Structural analysis

LEDs with embedded sub-µm stripes based on a dry etched SiN_x growth mask were investigated at the Central Electron Microscope Facility of Ulm University headed by Prof. U. Kaiser. TEM and STEM measurements were performed by J. Biskupek.

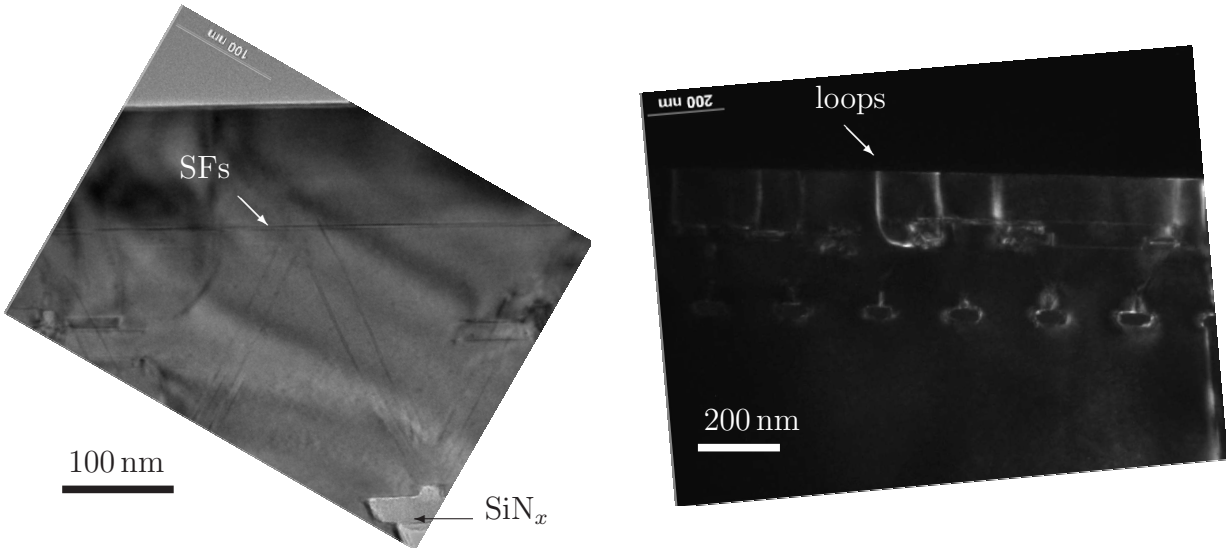

Fig. 5: TEM micrographs of embedded sub-µm sized GaN stripes with semipolar QWs. Stacking faults (SFs) originate at the ridges (left) and can lead to dislocation loops penetrating to the surface (right).

We observe the creation of stacking faults (SFs) at the ridges of the stripes which can cause dislocation loops penetrating to the surface, shown in Fig. 5. We assume that strain accumulates at the ridges during quantum well growth which is relaxed by the formation of stacking faults. The quantum wells themselves show an inhomogeneous thickness distribution and especially the later grown quantum well is not fully formed

along the facet, as can be seen in Fig. 6. We tentatively correlate the inhomogeneity of the quantum wells with the low homogeneity of the mask patterning still present when using the laser interference lithography.

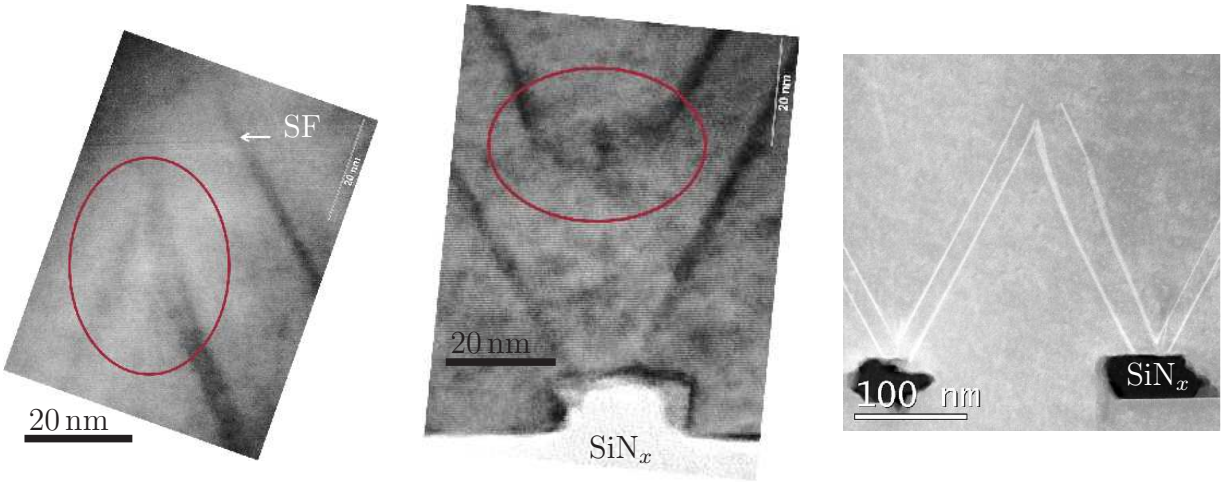

Fig. 6: TEM (left and middle) and STEM (right) micrographs of embedded sub-µm sized GaN stripes with semipolar QWs. The later grown quantum well is not fully formed during growth — especially at the top and bottom of the stripes (left and middle). An inhomogeneous mask patterning might cause severe QW inhomogeneity (right).

3. Conclusion and Outlook

LEDs with semipolar QWs have been manufactured and characterized. A strong influence of the embedded TiN_x mask was found leading to its replacement with SiN_x. Structural analysis revealed thickness inhomogeneities of the InGaN QWs and the creation of stacking faults at the ridges of the embedded sub-µm stripes.

In order to improve the homogeneity of the patterning, subsequent work will employ nanoimprint patterning with first experiments already ongoing. In order to prevent the formation of stacking faults, only a single quantum well will be used for future samples and an InGaN prewell is included to mitigate the abruptness of the strain gradient.

Acknowledgment

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HVPE Growth on MOVPE-Grown Semipolar $(11\bar{2}2)$ GaN

Marian Caliebe

In this article HVPE layers deposited on MOVPE-grown $(11\bar{2}2)$ *GaN are investigated. The properties of the MOVPE templates that are used for the HVPE experiments are described. HVPE overgrowth leads to a smoother surface and shows indications of a better crystal quality. For further improvements a HVPE growth temperature series was conducted.*

1. Introduction

Despite of long-lasting research and development, there are still challenges in the production of light-emitting diodes (LEDs) for general lighting and other applications. While excellent LEDs in the red and blue spectral range are commercially available yet, there is still a lack of highly efficient LEDs in the green to yellow range. In literature, this problem is referred to as the green gap.

For the GaN material system, one reason for the breaking down of the efficiency is the so-called quantum confined Stark effect (QCSE). Since today's LEDs are grown in the common [0001] (c-)direction, the internal polarization fields are perpendicular to the quantum wells. The cause of these internal fields are spontaneous and piezoelectric polarization. The reason for the latter is mechanical strain that increases with higher In incorporation in the quantum wells, which is necessary for long-wavelength emission. This leads to a local separation of electrons and holes in the quantum wells. Thus their lifetime increases and the radiative recombination rate decreases. This is discussed to be a major reason for the decrease of the device efficiency [1–3].

One way out could be the use of crystal planes with reduced polarization fields. Crystal planes perpendicular to the (0001) plane are called nonpolar, while all other planes in between are named semipolar.

High indium incorporation in nonpolar planes turned out to be very difficult, but is mandatory for long-wavelength emission. Also those planes contain high defect densities which give rise to nonradiative recombination. Thus the growth of semipolar crystal planes is favored [2, 4].

Today homoepitaxy is not an option because of deficient availability and high cost of semipolar bulk GaN wafers. Here, we focus on a heteroepitaxial approach, described in the dissertation of S. Schwaiger [4], to produce semipolar $(11\bar{2}2)$ GaN:

As shown in Fig. 1, $(10\bar{1}2)$ r-plane sapphire serves as a substrate. Trenches with c-plane-like side facets are etched into the substrate in a-direction of the sapphire. After masking

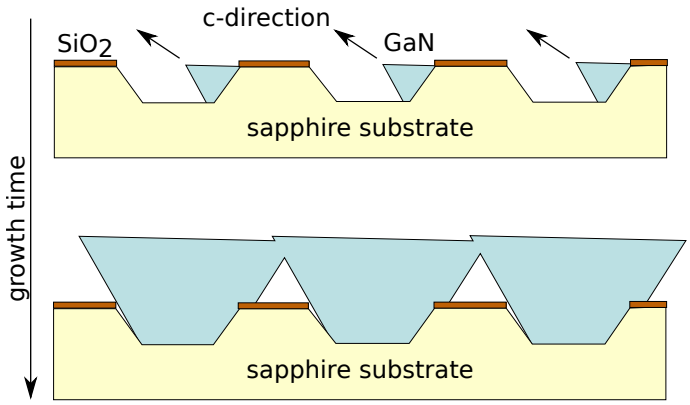

Fig. 1: Schematic of the production of $(11\bar{2}2)$ GaN substrates. During selective epitaxy, GaN stripes grow on the c-plane-like side walls of the trenches that have been etched into the sapphire substrate. After some time the individual stripes coalesce to a closed layer.

areas with SiO_2, selective growth with metalorganic vapour phase epitaxy (MOVPE) follows on the side facets of the trenches in the common c-direction with the following orientation: $c_{sapphire}||c_{GaN}$ and $a_{sapphire}||m_{GaN}$. r-plane sapphire is used because the angle of 57.61° between the $(10\bar{1}2)$ sapphire surface and the c-direction is very close to the angle of 58.41° between the $(11\bar{2}2)$ plane and the c-direction of GaN.

Eventually the single GaN stripes coalesce to a closed layer with $(11\bar{2}2)$ surface. Subsequently, we have overgrown these templates by hydride vapour phase epitaxy (HVPE). This method provides substantially higher growth rates. Hence thick layers can be grown, which should help to improve the crystal quality. There is also the possibility to produce freestanding GaN substrates by this method. The feasibility has been shown by Yamane et al. [7].

2. Experimental

The structuring of the r-plane sapphire substrates as well as the MOVPE growth are described in detail in T. Meisch's contribution to this Annual Report (p. 52 ff., Sect. 2.). For the templates used in the studies described below, the GaN buffer layer is grown at 1100°C. Both the SiN interlayer and the low-temperature top layer grown at 1000°C are included.

Properties of the MOVPE templates A template that has been grown under the above described conditions shows full widths half maxima (FWHMs) of high-resolution X-ray diffraction rocking curves (HRXRD RCs) of 265" and 430" for the symmetric $(11\bar{2}2)$ reflection parallel and perpendicular to the c-direction, respectively and 337" for the asymmetric $(11\bar{2}4)$ reflection. Atomic force microscopy (AFM) measurements show a surface roughness of 82 nm (root mean square (RMS)) on an area of $20 \times 20\,\mu m^2$.

2.1 HVPE overgrowth

For further improvements the samples have been overgrown by HVPE with the following conditions: growth temperature $T = 890°C$, pressure $p = 900\,\text{hPa}$, V/III ratio = 17.5 and growth time $t = 60\,\text{min}$. This experiment was done along the parameters described in [4]. In Sect. 2.2 they have been varied for further improvements.

HVPE results and comparison to the MOVPE template Scanning electron microscope (SEM) investigations of the cross-section (Fig. 2) show a clear material contrast between the MOVPE and the HVPE layer. The growth rate under the above described conditions is $12.3\,\mu\text{m/h}$.

The FWHM of the HRXRD rocking curve of the symmetric $(11\bar{2}2)$ reflections (parallel and perpendicular to the c-direction) dropped to 185" and 264", respectively, though the FWHM of the asymmetric $(11\bar{2}4)$ reflection increased to 365".

The AFM results are depicted in Fig. 3. The MOVPE template shows a sawtooth-like surface. The origin is the coalescence of the single GaN stripes and the misalignment of the c-directions of sapphire and GaN. After HVPE overgrowth, the surface turned into a bubble-like structure with reduced roughness of 42 nm (RMS) on an area of $20 \times 20\,\mu\text{m}^2$.

2.2 HVPE temperature series

In order to achieve a higher growth rate and to investigate the influence of the growth temperature, the experiment has been repeated with increased temperatures of 930°C and 970°C.

Direct results As shown in Fig. 4, the growth rate could only be increased a little bit at 930°C. At 970°C the growth rate drops again. The higher growth rate seems to influence

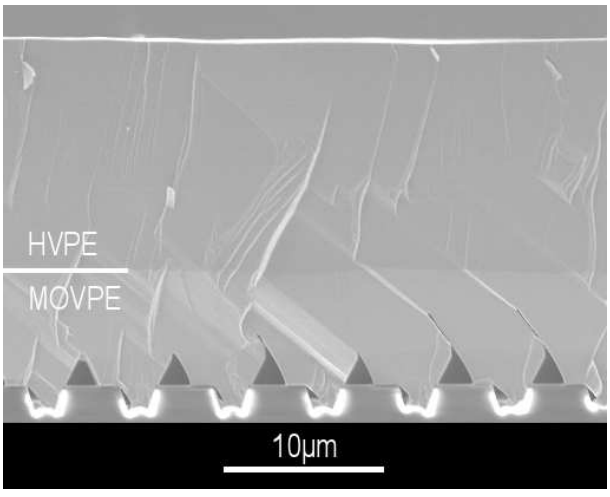

Fig. 2: SEM in-lens image of the HVPE sample. A clear material contrast between the HVPE and MOVPE layer is visible.

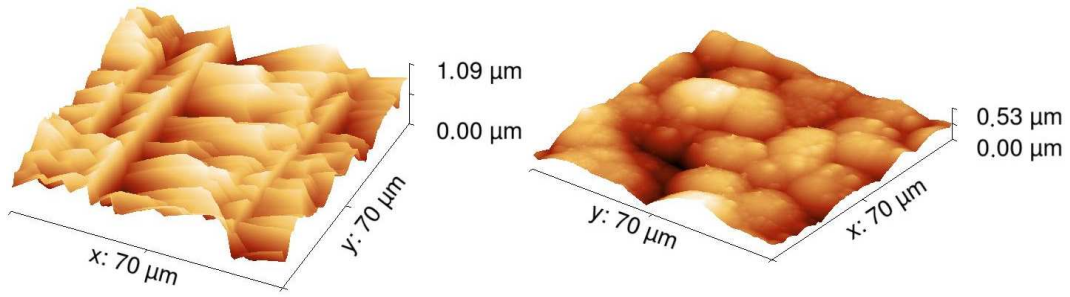

Fig. 3: AFM measurement of the MOVPE (left) and HVPE sample (right). With HVPE the sawtooth-like surface of the MOVPE sample became a bubble-like structure with reduced roughness.

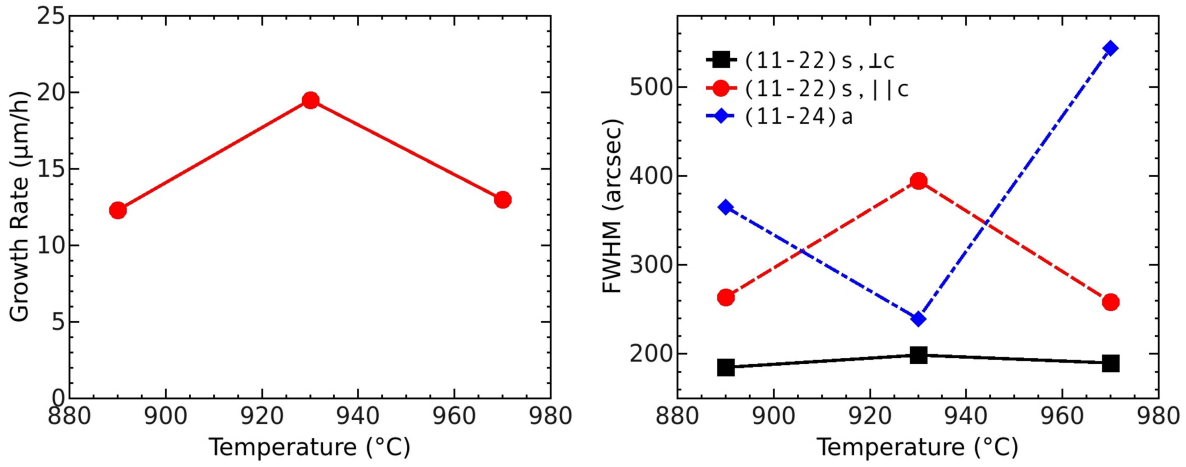

Fig. 4: HVPE growth rate in $[11\bar{2}2]$ direction (left) and FWHM of HRXRD RCs over temperature (right).

the crystal quality in a negative way. The FWHMs of the HRXRD RCs of the $(11\bar{2}2)$ reflections both increase. Interestingly the FWHM of the $(11\bar{2}4)$ reflection is decreasing, so no clear conclusion can be drawn out of this data. Also the normal process variation has to be considered.

The AFM measurements show more clear results (Fig. 5). The surface roughness decreases with higher temperatures. For a fair comparison, the area used to determine the RMS value has been increased to $50 \times 50\,\mu m^2$.

Hillocks On all HVPE samples, huge hillocks emerged (Fig. 6). They are randomly distributed on the wafer with a slightly higher density at the wafer edge. The hillocks have a height of approximately 20 µm, length of 145 µm and width of 75 µm. They are smoothing iron shaped and are all oriented in the same direction perpendicular to the trenches in the sapphire in +c-direction. An electron backscatter diffraction (EBSD)

measurement revealed that they are grown monocrystallinely on the GaN layer. The origin is unknown at present and will be further investigated.

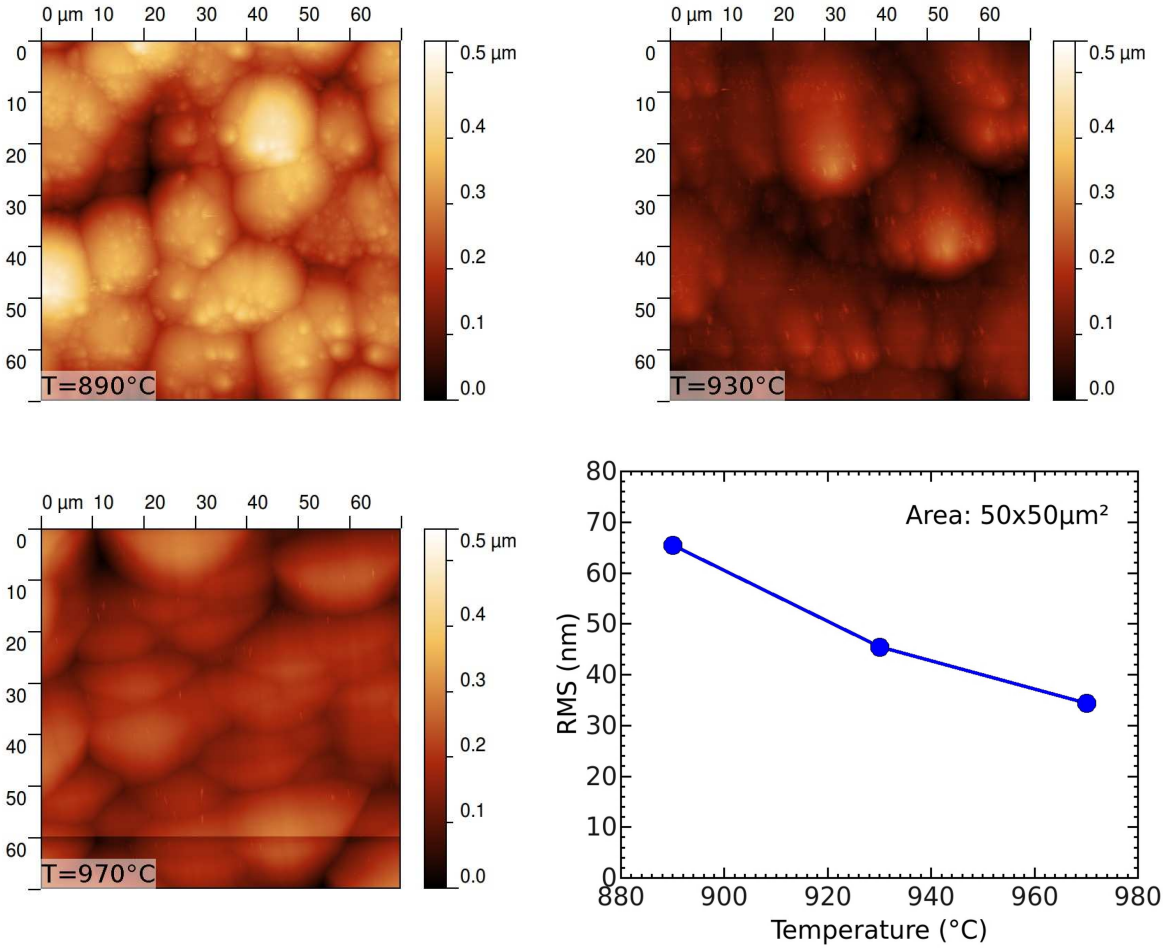

Fig. 5: AFM measurement of the samples grown at 890°C, 930°C and 970°C. Bottom right: the surface roughness decreases with higher temperature.

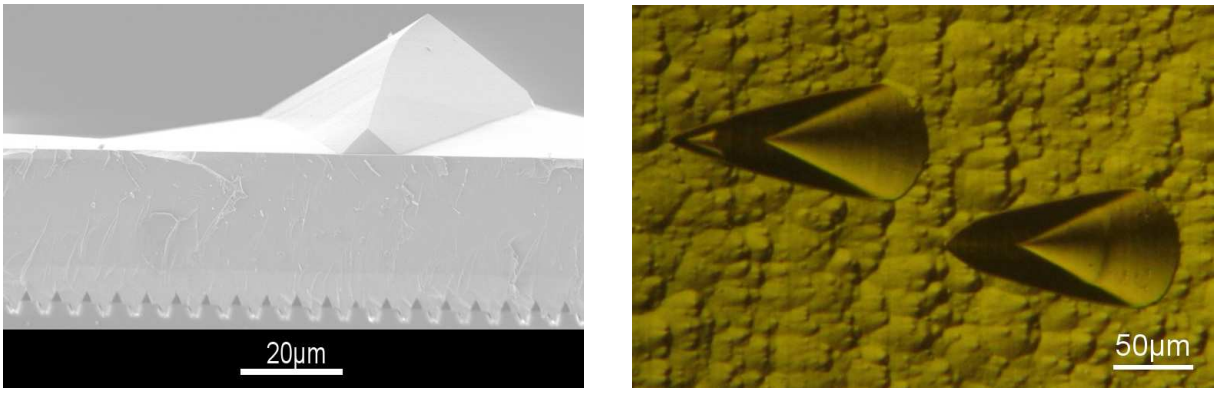

Fig. 6: Typical appearance of the hillocks observed on all HVPE samples. Left: SEM, right: optical microscope.

PL and CL measurements In Fig. 7 (left), the photoluminescence (PL) spectra of the HVPE samples are depicted. As a reference the PL spectrum of the MOVPE template has been inserted in this graph, too. It was necessary to scale it down by a factor of approximately 100, since it has a much higher intensity and was measured with another sprectrometer. The peak at approximately 3.48 eV can be assigned to the donor-bound exciton (D^0X) transition and the peak at 3.46 eV might be related to acceptor-bound excitons (A^0X). The reason for the peak at approximately 3.42 eV might be basal plane stacking faults (BSF). We observed a slight shift of the D^0X peak energy, which is probably due to strain differences caused by varying growth temperatures and layer thicknesses. The peaks of the HVPE samples at lower energies are not as distinct as the peaks of the MOVPE sample. Also a high-energy peak above 3.5 eV was observed on all HVPE samples. The MOVPE sample does not show this peak. It is important to mention that the energy of the maximum shifts with higher growth temperatures to higher energies and the peak gets broader.

To investigate its origin, cathodoluminescence (CL) measurements of the cross-section have been performed. Also here a clear material contrast between the HVPE layer and the MOVPE layer was detected (Fig. 8). Local CL spectra show the high energy-peak that was measured with PL, too. As can be seen in Fig. 7 (right), it clearly belongs to the HVPE layer.

To ensure that no Al content is causing this peak, a secondary ion mass spectrometry (SIMS) measurement was done. The Al concentration was below the detection limit.

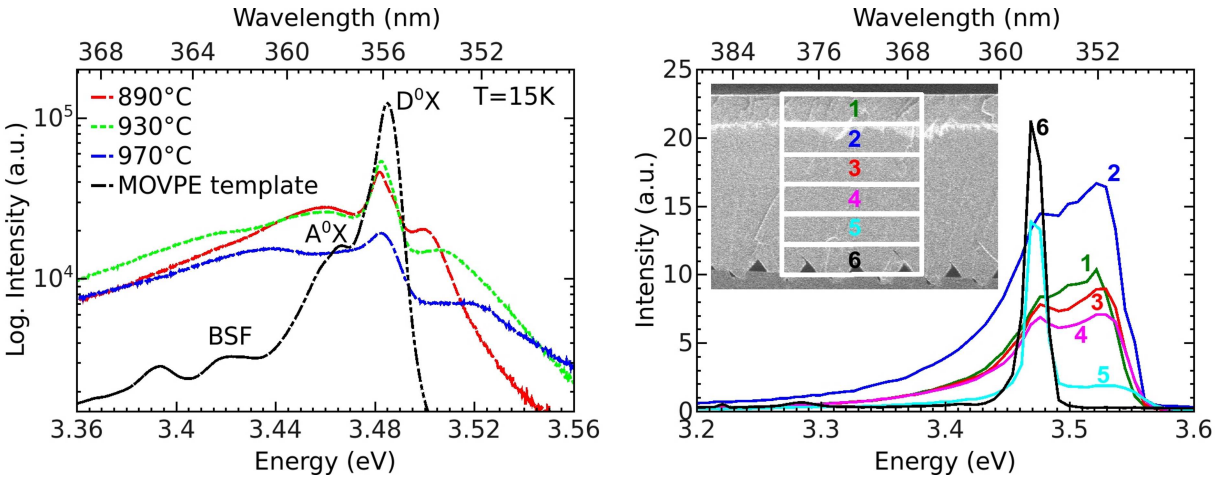

Fig. 7: Left: PL spectrum of the HVPE samples and downscaled spectrum of a MOVPE template. A high-energy peak above 3.5 eV of unknown origin that shifts to higher energies with higher growth temperatures was observed. Right: Local CL spectra. The high-energy peak originates from the HVPE layer and was not found in the MOVPE layer.

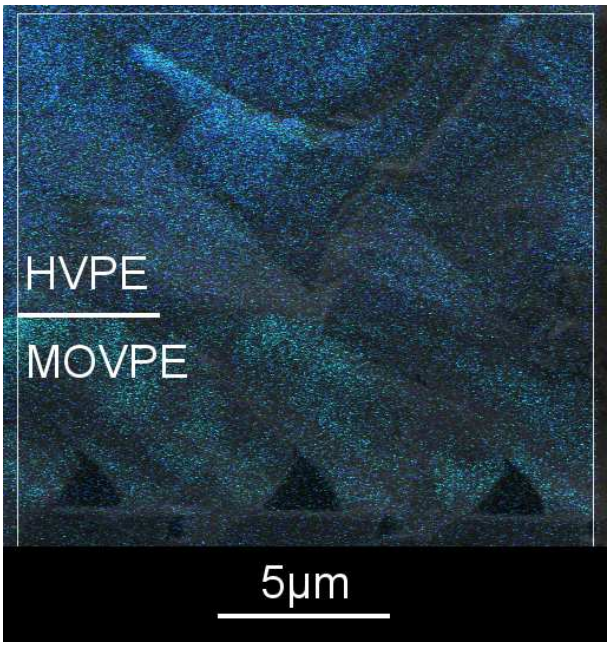

Fig. 8: CL image of the cross-section of the sample grown at 930°C. A clear material contrast is visible between the HVPE layer (top) and the MOVPE layer (bottom).

3. Conclusion

A method to produce semipolar $(11\bar{2}2)$ oriented GaN on r-plane prestructured sapphire substrates was shown.

GaN templates are produced by MOVPE. For our investigations, the MOVPE templates were overgrown by HVPE and compared to the previous MOVPE templates. Finally, a HVPE temperature series was performed to improve the growth conditions.

Compared to the MOVPE template, the FWHMs of the HRXRD rocking curves of the $(11\bar{2}2)$ reflections improved, whereas the $(11\bar{2}4)$ peak got worse. A considerable change in the surface morphology was observed: the sawtooth structure that is common for MOVPE templates turned into a bubble structure with highly reduced roughness.

For further improvements, the growth temperature of the HVPE layer was increased. Only minor improvements of the low growth rate were achieved at the expense of crystal quality. However, it could be shown that the surface roughness decreases with higher temperatures.

Two further phenomena, which are unexplained yet, were observed: on all HVPE samples, huge hillocks emerged. For later device processing, their formation must be avoided. Also a high-energy peak of unknown origin above 3.5 eV was observed in PL and CL measurements. Local CL spectra revealed that this peak belongs to the HVPE layer. Its origin needs further investigations.

Acknowledgment

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Influencing the Bow of Thick Hydride Vapor Phase Epitaxial GaN by Prestraining MOVPE Templates

Martin Klein

A major challenge that arises when growing GaN substrates in a single run process is the remaining curvature of the freestanding material after the removal of the foreign substrate. For a long time the dislocation density gradient has been suspected to be the cause. However, by conducting etching experiments, we have found that this cannot be the only reason. We postulate that the initial strain situation of the MOVPE template can have a big influence on the bowing of HVPE samples and on the remaining curvature of separated GaN layers. By investigating accordingly grown samples, we present proof of this assumption.

1. Introduction

GaN has gained a very significant share in the semiconductor market over the last years. Applications extend from high-power, high-frequency transistors [1] and solid state lighting by GaN-based light emitting diodes (LEDs) [2] to laser diodes in the blue and ultraviolet emission regime [3]. Most of these devices are epitaxially grown on foreign substrates such as sapphire, silicon-carbide and silicon. By this heteroepitaxial approach defect densities in the range of $10^8\,\mathrm{cm}^{-2}$ can be achieved [4]. Although the number of defects is quite high, this method is most commonly used for LEDs and transistors because of its low cost and high availability. In laser diodes, however, high defect densities result in short lifetimes and low efficiencies, so that low defect density GaN substrates are urgently needed [5].

A quite simple approach to produce GaN substrates is using hydride vapor phase epitaxy (HVPE) to grow thick layers. These layers are subsequently separated from the substrate. A typical layer thickness of freestanding GaN by HVPE is 1 mm, which can be reached in about 10 hours of growth. In order to grow such layers in HVPE, foreign substrates are needed, so that many problems connected with heteroepitaxy still arise. During the growth of thick layers, nearby dislocations may annihilate each other. By this effect defect densities on the surface of the thick GaN layer in the range of $10^6\,\mathrm{cm}^{-2}$ can be achieved when growing on templates inheriting defect densities in the $10^8\,\mathrm{cm}^{-2}$ regime [6]. When we reach about 1 mm of layer thickness, we stop the growth and start to cool down the reactor. During this cool-down, great stress forces build up in the wafer due to different thermal expansion coefficients of layer and substrate. By carefule usage of these forces and a specially designed interlayer close to the sapphire substrate, we manage to separate the GaN layer from the substrate [7].

A more severe problem arising with heteroepitaxy, is the curvature of the wafer due to differences in the thermal expansion coefficients of substrate and grown layer. With the GaN layer removed from the substrate one would expect that the layer is now totally relaxed and no bowing remains. In fact photo luminescence measurements confirm that the material is macroscopically relaxed. However these layers still experience some bowing. In [6] F. Lipski and F. Scholz showed that this bowing can't be caused by a gradient of the dislocation density in the material alone. Instead they postulated that the strain situation created at the beginning of the growth of the template could have a great influence on HVPE growth and the bowing of still attached and separated thick GaN layers. During the last year we conducted several growth runs to prove this postulation and to optimise the template conditions to obtain layers with lower curvature values.

2. Prestraining MOVPE Templates

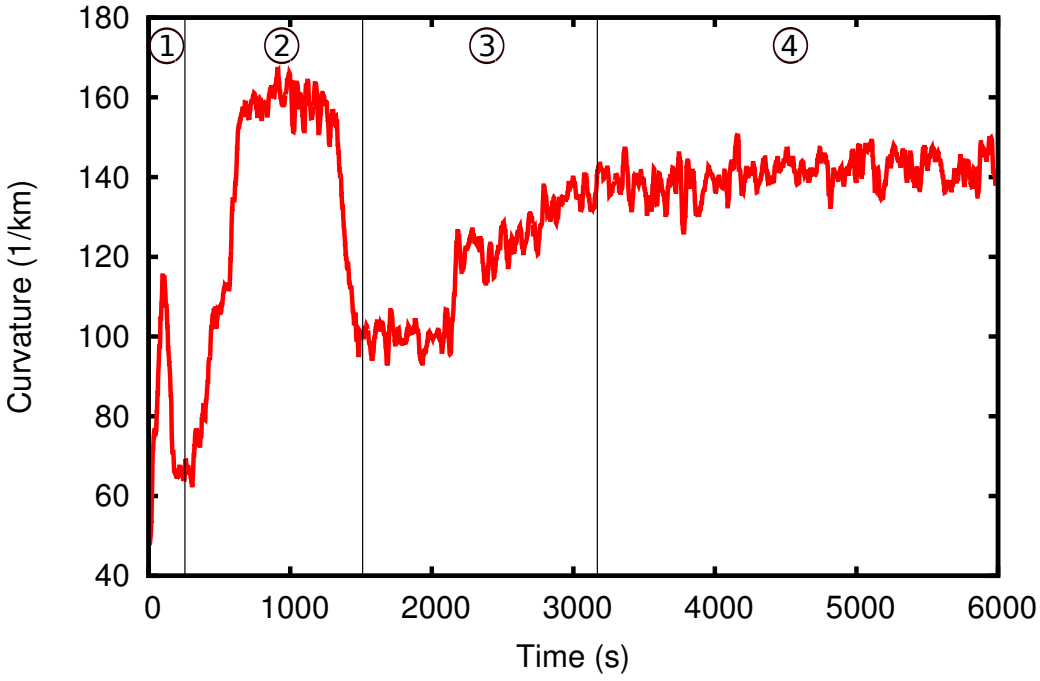

Fig. 1: *In-situ* curvature measurement during MOVPE growth. Sections 1–4 contain different growth steps.

When comparing the remaining bow of freestanding samples with the initial bow of the templates that have been used to grow these layers, no obvious connection can be seen. However, we found some evidence that the nucleation layer and some interlayers can have an influence on the strain of the layer grown on top. To control this strain situation we used a combination of our oxygen-doped aluminium–nitride (AlN) nucleation layer and a submonolayer of SiN_x, normally used for defect reduction. We figured out that by varying the thickness of the GaN buffer between those layers, it is possible to directly influence the strain situation. This could be confirmed by photoluminescence (PL) experiments [4]. The

peak with the highest energetic position could be found when we deposit the SiN_x directly on top of the nucleation layer, marking the compressive end of the possible strain created by this three-layer system. The thicker we grow the GaN buffer between nucleation and SiN_x layer, the lower the PL emission energy, indicating that the strain is being moved towards a more tensile state [4].

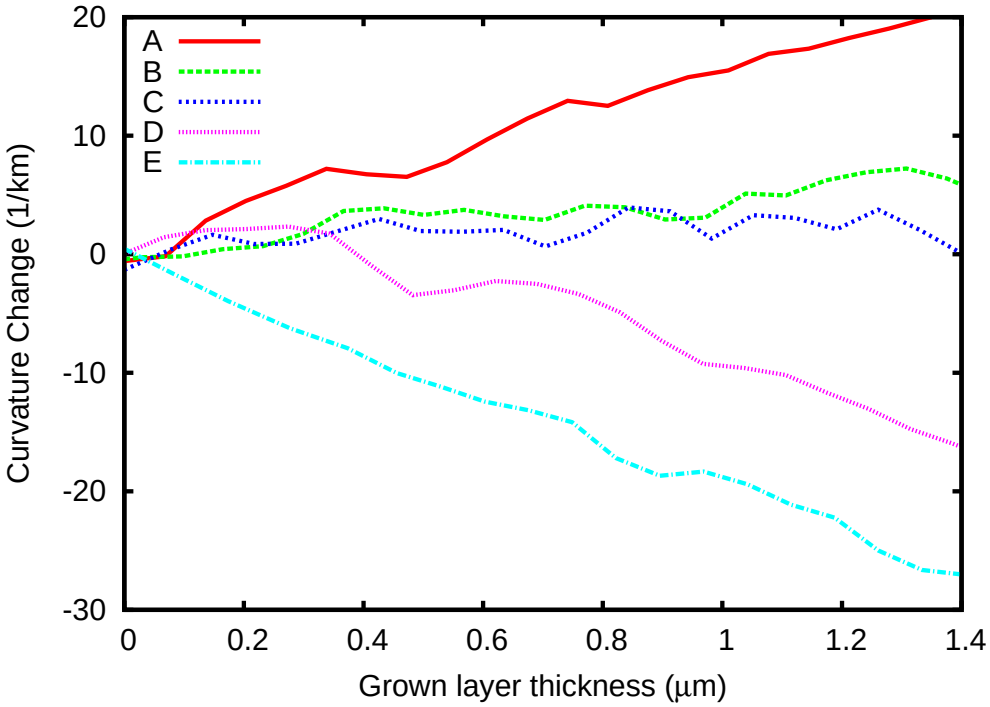

Fig. 2: *In-situ* curvature measurement in MOVPE. Curves A–E have been measured during template growth runs with different growth parameters.

Our metal organic vapor phase epitaxy (MOVPE) machine is equipped with a LayTec Epicurve to monitor curvature during growth. With this tool we can determine the wafer curvature by measuring the distance of two reflected laser spots. Therefore we see the influence of process changes already during growth. Figure 1 shows a typical *in-situ* curvature measurement curve, taken during one of our template runs in our MOVPE. In section **1** we see that the wafer already has some initial curvature. This is a statistical value due to the sapphire fabrication process, and some curvature at this point normally can't be avoided. Subsequently we see a spike in section **1** which is a measurement artifact caused by pumping and purging the reactor. In section **2** the sapphire is heated up in a hydrogen ambient for thermal cleaning. After cooling down to growth temperature we deposit the nucleation layer, a GaN buffer and the SiN_x interlayer in section **3**, before we create a closed and flat layer in section **4**. For more compressively strained layers we observe a downward curve in this section, so the curvature develops towards a convex shape. For more tensile strained layers the curve goes upward, developing a more concave shape. We believe that for freestanding layers the best situation is when the curvature doesn't change at all, therefore our goal was to find the right buffer layer thickness to

achieve this state.

Figure 2 shows a more detailed picture of section **4** from Fig. 1 from some different template runs. Sample A includes no SiN_x interlayer. Therefore this curve marks the most tensile strain state that can be achieved by this method. Even higher tensile strains can be achieved by using a GaN-based nucleation layer instead of our AlN-based nucleation. Sample B has been taken during growth of our standard process, optimised for a low etch pit density (EPD). This sample includes a 300 nm thick buffer layer between nucleation and SiN_x interlayer. Sample C has a thinner GaN buffer and is close to be perfectly optimized for further HVPE growth, almost no change of the curvature value can be seen. If we reduce the buffer layer further, we obtain a curve as shown for sample D. This sample already shows a quite compressive behaviour. Leaving the buffer layer out entirely, we receive the curve named sample E, which marks the most compressive strain state possible with the combination of oxygen-doped aluminium–nitride nucleation layer and a sub-monolayer of SiN_x as an interlayer.

2.1 Influence on thin HVPE layers

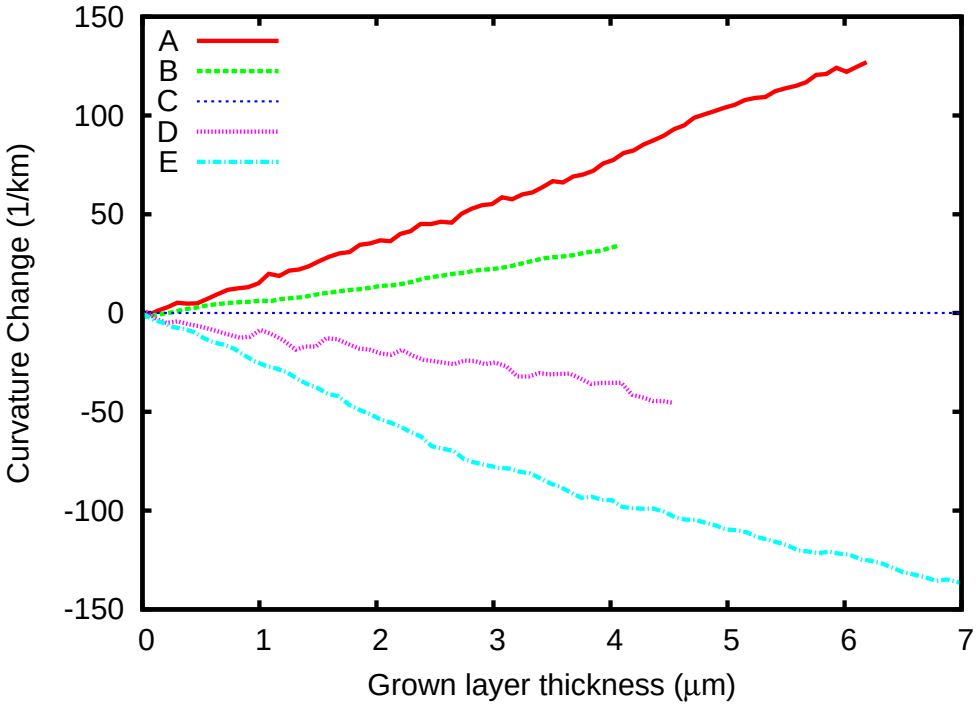

Fig. 3: *In-situ* curvature measurement like in Fig. 2 but during overgrowth in HVPE. Samples A–E correspond to the samples in Fig. 2.

The samples shown in Fig. 2 have been overgrown by 65 µm of GaN in HVPE. The *in-situ* curvature measurements of the first micrometers of growth of these HVPE runs can be seen in Fig. 3. Unfortunately we don't have any real data for curve C as the *in-situ* measurement was not available in this run. For all other samples we can see that the

curvature evolution during MOVPE and HVPE growth is more or less the same for a given sample.

Next we measured the room temperature curvature of the resulting wafers. In order to get these values, x-ray diffraction (XRD) rocking curve scans have been taken at several positions along the wafer diameter. The curvature can then be calculated from the distance between the measurement spots and the difference in the respective rocking curve angles. Our measurement results are shown in Fig. 4. The ordering of the samples is as we would expect from the *in-situ* measurements. The sample with the strongest tensile development shows the smallest curvature, whereas the sample with the strongest compressive development shows the largest curvature. As some edge effects seem to influence the curvature of our wafers we always take center value as figure of merit. In case of sample A the measurement range is significantly shorter than for all other samples. Because of the strong tensile strain in the GaN layer, the overall stress became too strong during cool-down and the wafer cracked at the edge several times.

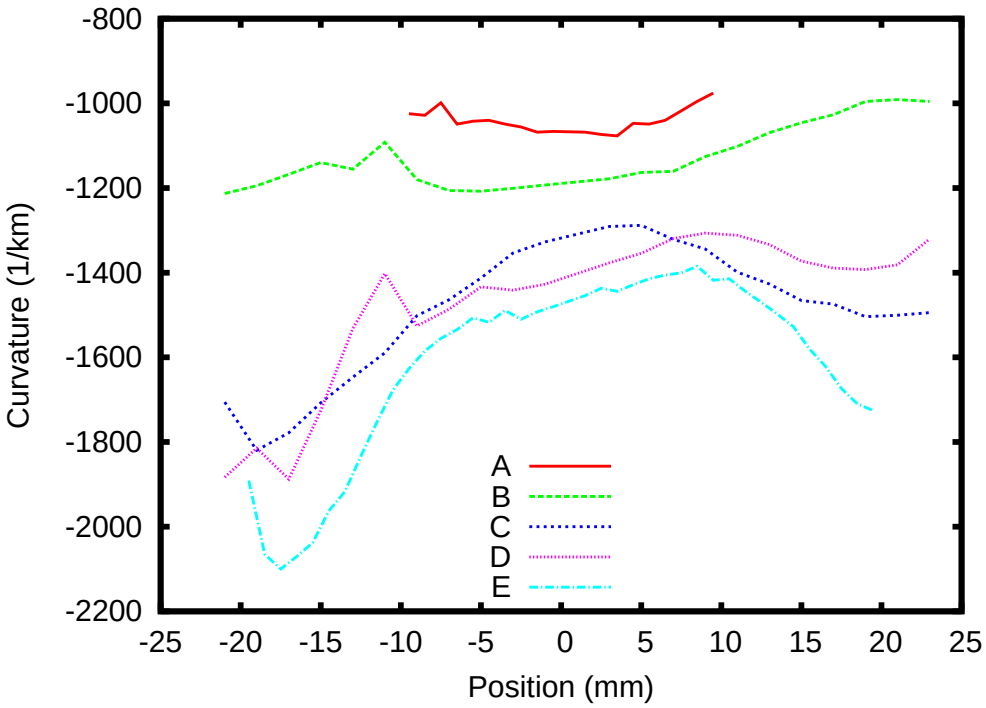

Fig. 4: Room temperature *ex-situ* curvature measured by x-ray diffraction along the wafer diameter of 65 µm thick HVPE samples. Samples A–E correspond to the samples in Fig. 2 and Fig. 3.

2.2 Influence on freestanding GaN layers

In order to investigate the influence of strain-optimized samples on self-separated layers, we grew a set of freestanding samples with old and new templates, stopping growth at different thicknesses for self-separation. The curvature values of former samples with EPD

optimized growth steps are shown as squares in Fig. 5. We can see that for these samples the curvature is highly dependent on the layer thickness. The reason herefore is given in the next paragraph. The triangles are marking the curvature values of the curvature optimised templates at growth temperature. Next to the triangles we find the curvature values of the corresponding freestanding samples, represented by light dots. The small curvature difference of template and freestanding layer confirms that the curvature is not undergoing big changes during HVPE growth.

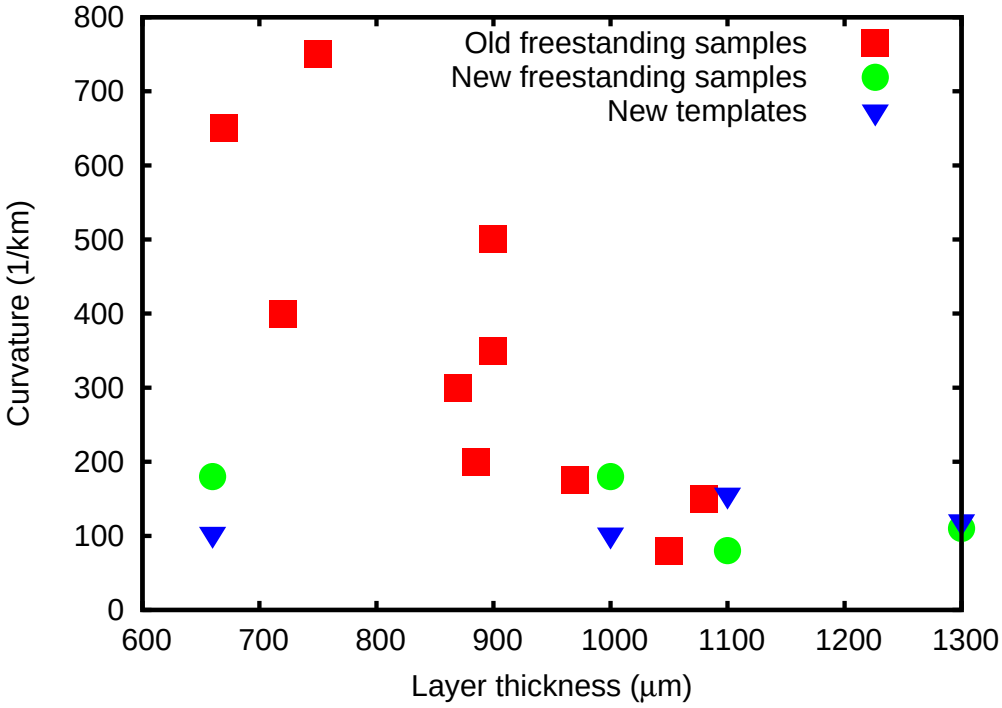

Fig. 5: Remaining curvature of self-separated HVPE, samples separated at different thicknesses.

Templates optimised for low EPD values are generally tensile strained. This leads to a growing curvature in the beginning of HVPE growth. The curvature value increases up until the GaN has about the same thickness as the sapphire substrate underneath. When we grow thicker than this, the curvature gets reduced again. When we grow on a bent surface the material would need to to change its strain state in order to reproduce the same curvature in the next monolayer. Instead the material produces a certain low amount of new dislocations to keep the former strain. By this mechanism some curvature is frozen into the material. When we now separate the layer at a certain thickness, this frozen curvature remains in the material. To reduce the remaining bow one could growth thicker layers before separating. But if we grow significantly thicker than 1 mm, the material is not separating at the intended position. Instead, separation occurs roughly 200 µm above the separation layer. Therefore it is not possible to reduce the curvature to zero with these templates. As for the strain optimized samples, we are able to set the remaining curvature by influencing the curvature of the template at growth temperature, regardless of the thickness during separation. A simple approach to achieve this would be by using

uncurved or intentionally curved sapphire wafers, which inherit a concave curvature rather than the usual convex curvature. Fortunately, a method has been published recently on how to create such sapphire substrates [8] and we are planning to grow samples on such substrates in the near future.

3. Conclusion and Outlook

A big problem that still remains when producing GaN wafers in a single wafer process is the remaining curvature of the separated layers. In the bygone year we were able to establish a template process that holds out the prospect of effectively handling this problem. When using our former standard templates, the curvature during growth is dependent on the layer thickness. By optimising the growth sequence in the first stage of our MOVPE process, we were able to stop the development of the wafer curvature in subsequent growth steps. This also holds true for a subsequent overgrowth in an HVPE machine. After establishing this template process we investigated the HVPE growth on templates with different values for the change of the curvature during the process. In these experiments we got low curvature values for all separated layers grown on our new templates, regardless of the thickness of the separated layer. For all other samples, the remaining curvature depended on the thickness of the separated layer and in most cases significantly larger than the remaining curvature of layers grown on optimised templates.

In the near future we intend to reduce the remaining curvature in separated layers by reducing the initial curvature of our MOVPE templates. A very promising parameter to start with is the initial curvature of the sapphire substrates. Only recently a company has developed a process to influence the initial curvature of sapphire wafers [8], so that corresponding substrates are now available for scientific purposes.

Acknowledgment

I thank I. Schwaiger for preparing the separation templates and T. Meisch for finding the right buffer thickness for the optimized templates. This work was financially supported by the German Federal Ministry of Education and Research as part of the project “TeleGaN”.

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Growth Investigations of Nitrogen-Polar GaN Nucleation Layer Templates

Mohamed Fikry

This study aims at achieving highly crystalline and smooth Nitrogen-polar (N-polar) GaN layers deposited on c-plane sapphire by metal organic vapor phase epitaxy (MOVPE). The influence of nitridation, temperature and V/III ratio on the polarity, quality and coalescence of GaN is systematically investigated. It was observed that the initial nitridation of sapphire before GaN growth is critical for achieving N-polar growth and improving the crystal quality. Moreover, higher GaN deposition temperatures (above 1100°C) result in lower coalescence and growth of vertical micro-hexagonal structures with a large degree of N-polarity, while lower temperatures (below 950°C) resulted in a coalesced layer but lower degree of N-polarity and crystal quality. Growth under a low V/III ratio (below 50) at a temperature of 1000°C showed complete coalescence with a layer thickness of 170 nm and a linewidth of 20 meV for the GaN band-edge emission in low temperature photoluminescence, whereas a higher V/III ratio of 1100 resulted in GaN structures separated from one another (lower degree of coalescence). Finally, selectively grown vertical GaN micro-rods on masked nitridated sapphire proved to be exhibiting mainly N-polar crystal orientation.

1. Introduction

Group III-nitrides have a polar asymmetry along the c-axis of their hexagonal wurtzite crystal structure [1]. As confirmed by the larger number of publications, most light emitting diodes, laser diodes, and high electron mobility transistors have been developed on Ga-polar GaN templates. Recently, N-polar GaN films have attracted increasing attention. The flipped spontaneous and piezoelectric polarizations for N-polar GaN films can be a further degree of freedom for the design in various devices. The advantages include higher chemical surface reactivity for sensor applications [2], lower gate leakage current in N-polar GaN/AlGaN/GaN HEMTs [3] as well as enhancement of vertical growth of selectively grown structures on masked substrates [4]. The latter point could be utilized for the realization of well ordered upright GaN nano- and micro-pillars. The initial nitridation of the sapphire substrate and buffer layer growth have been identified as the main differences in polarity of the GaN films [5]. Growth initiation using a thin GaN or AlN layer at lower temperatures have been reported to result in GaN films with Ga polarity [6]. However, if the sapphire substrate is exposed to the N precursor at high temperatures prior to GaN growth leading to the formation of a thin AlN surface layer [5], typically N-polar GaN films result [7]. In this study we investigate the influence of temperature, nitridation and V/III ratio on the polarity, quality and coalescence of thin GaN nucleation layers (around 170 nm) on c-plane sapphire by metal organic vapor phase epitaxy (MOVPE).

2. Experimental

A reference layer template identified for our experiments for the systematic variation of growth parameters is described in Table 1. Trimethylgallium (TMGa) and ammonia (NH_3) were used for the deposition of GaN layers. Before the growth, all sapphire wafers were heated under H_2 flow for 5 minutes at 1110 °C for thermal cleaning of the surface. Then nitridation of the surface was performed under 67 mmol/minute ammonia flow for 7 minutes at the same temperature of 1110 °C. GaN deposition took place as the subsequent step (Table 1). To verify the polarity of our layers, the samples were wet chemically etched in an aqueous KOH solution (5 mol/liter) at 80 °C for 50 minutes [4]. Low temperature photoluminescence (LT-PL) with a laser spot size of 150 µm was used for determination of the layer quality in addition to high resolution X-ray diffraction (only for totally coalesced layers).

Table 1: Growth parameters for GaN grown directly on nitridated sapphire. Growth temperature and V/III ratio have been varied within the investigations.

Growth parameter	
Time (min.)	10
Pressure (hPa)	100
Temperature (°C)	920–1110
V/III	45–1000
Carrier gas	N_2/H_2 (1:2)

3. Effect of Nitridation

Our first question was to check the effect of nitridation on the polarity and quality of our layers. The growth procedure described in the experimental section using a GaN growth temperature of 1000 °C and V/III ratio of 120 was applied twice, namely, with and without a nitridation step prior to GaN growth. The layer grown without nitridation (Fig. 1 (b)) had a reduced degree of coalescence compared to its counterpart grown on a nitridated sapphire (Fig. 1 (a)). But most importantly, reconsidering the afore-mentioned comparison, very little of the grown GaN was etched after the KOH test for the layer without nitridation (Figs. 1 (c) and (d)). This indicated a clear influence of the nitridation step on the etching rate in the aqueous KOH solution and hence the chemical reactivity of the surface (as a verification sign for N-polarity of the layer). In addition, skipping the nitridation step resulted in lower crystal quality due to the very strong broad yellow luminescence and the broad GaN band-edge luminescence with 142 meV linewidth (Fig. 2). Grandjean et al. [5] observed a strong variation of the surface lattice parameter of the sapphire to confirm the existence of the AlN layer using reflection high-energy electron diffraction. This surface layer also was confirmed to facilitate the nucleation of GaN

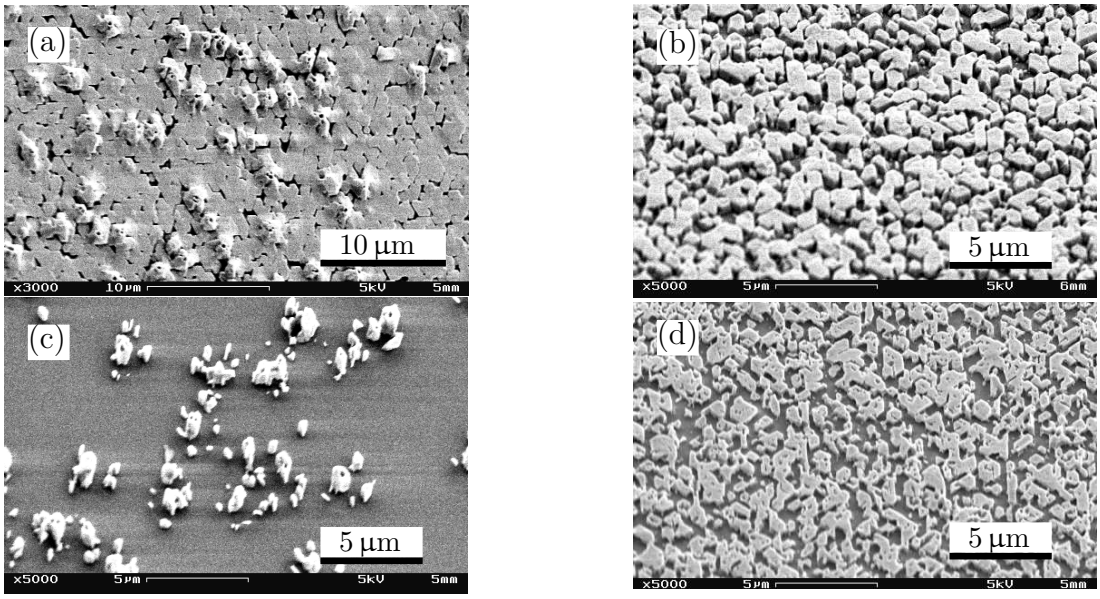

Fig. 1: Scanning Electron microscope (SEM) pictures of GaN grown for 10 minutes directly on sapphire at 1000 °C with and without a nitridation step prior to GaN growth, before (a,b) and after (c,d) etching in aqueous KOH solution (5 mol/liter) at 80 °C for 50 minutes, respectively.

on such a nitridated surface rather than on bare sapphire, thus enhancing its respective crystal quality and dictating the polarity orientation of the overgrown crystal. Future work is planned to check the influence of duration, temperature and ammonia supply during the nitridation process on the orientation and crystal quality of the GaN layers.

4. Effect of Temperature

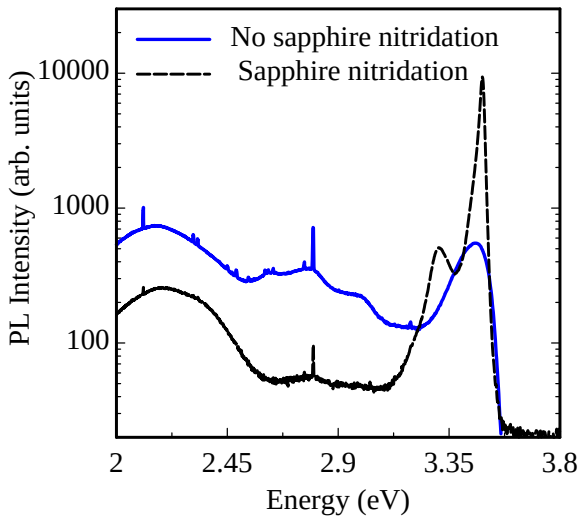

Fig. 2: LT-PL spectrum of GaN grown for 10 minutes directly on sapphire with and without a nitridation step at 1000 °C.

A set of three samples grown at the temperatures of 1110 °C, 1000 °C and 920 °C were grown using the parameters shown in Table 1 with a V/III ratio fixed at 120. As shown in

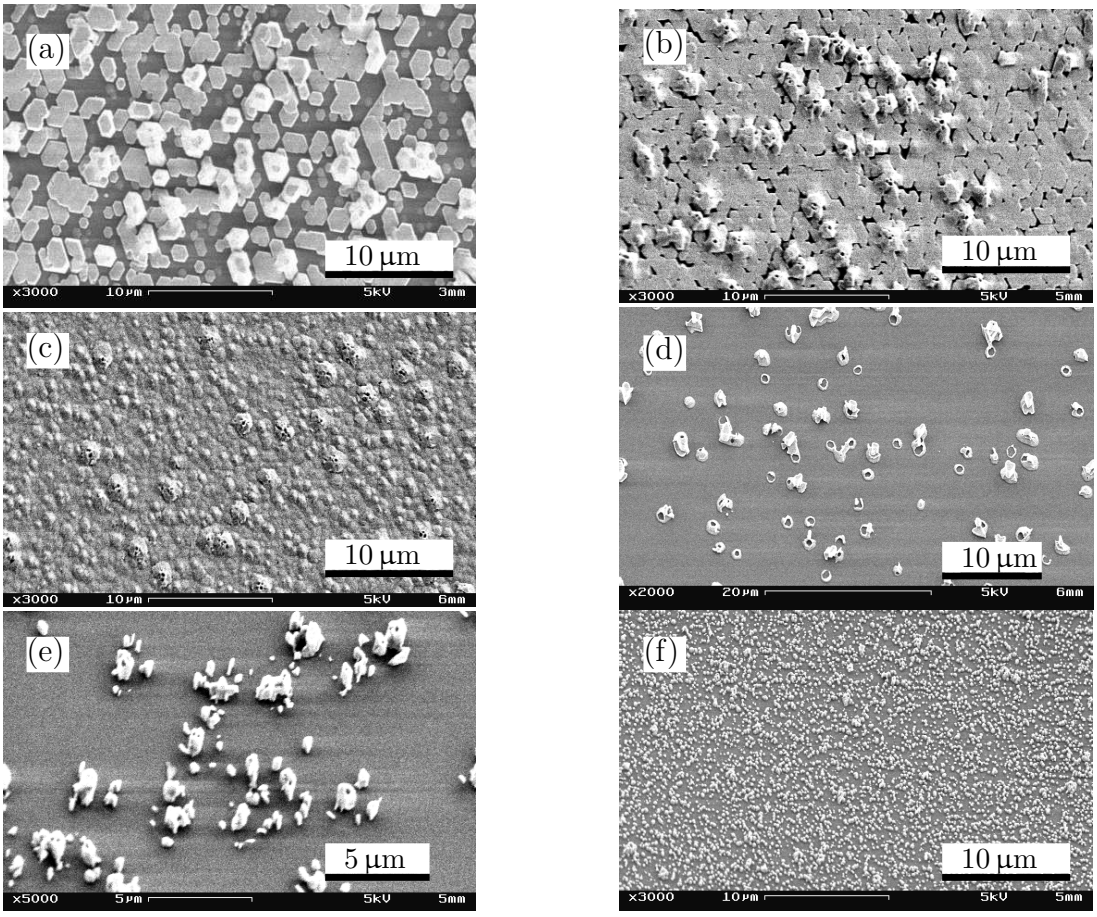

Fig. 3: SEM pictures of GaN grown for 10 minutes directly on nitridated sapphire at 1110 °C (a), 1000 °C (b) and 920 °C (c) before and after etching in aqueous KOH solution (5 mol/liter) at 80 °C for 50 minutes (d), (e) and (f), respectively.

Fig. 3 (a), the growth at 1100 °C was characterized by a large number of separated GaN micro-hexagonal structures. Also, the coalescence of the layer showed an inverse relation with temperature (Figs. 3 (a), (b) and (c)). The degree of N-polarity of the grown GaN, however, showed more N-polar nature at higher temperatures due to the observed higher etching rate of the structures (Fig. 3 (d)). In LT-PL (Fig. 4), we were able to observe the narrowest band-edge emission of GaN with 25 meV for the sample grown at 1000 °C. A second weak-intensity peak at 3.33 eV was observed for the afore-mentioned samples that is assumed to be related to prismatic stacking fault luminescence [8]. The sample grown at 920 °C showed the weakest band-edge and the strongest yellow luminescence intensities, respectively, indicating a poorer material quality. The yellow luminescence is believed to originate from either atomic crystal vacancies or carbon impurities (as reported in [9], pp. 19–34 and the references therein). This is expected to be due to the lower degree of atomic surface mobility of atoms to find their energetically favored sites in the crystal as well as the reduced precursor cracking efficiency at lower temperatures. We also believe that at temperatures above 1100 °C, a higher rate of atomic desorption from the surface results hindering the layer coalescence. This is in addition to the fact that sapphire nitridation as the formation of a relaxed AlN layer [5] (as described in

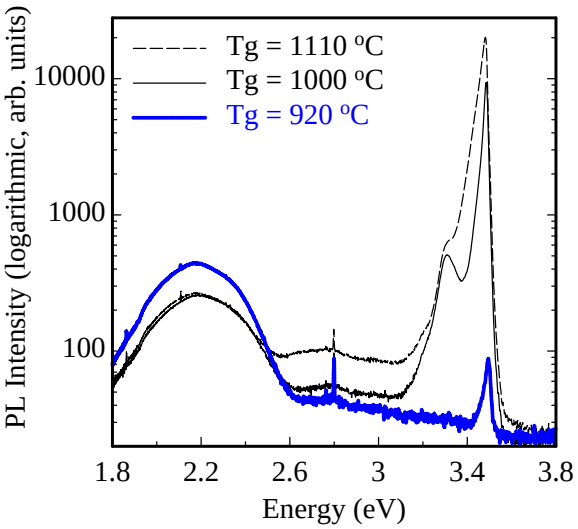

Fig. 4: LT-PL spectra of GaN grown for 10 minutes directly on nitridated sapphire at growth temperatures (Tg) of 1110, 1000 and 920 °C.

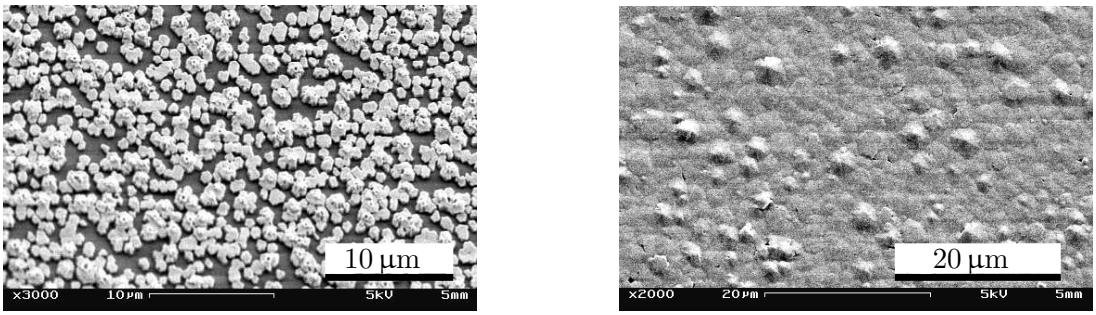

Fig. 5: SEM pictures of GaN grown for 10 minutes directly on nitridated sapphire at 1000 °C with V/III ratios of 1100 (left) and 45 (right).

the previous section) is believed to be constantly effected even during growth at this high temperature regime. Hence, it dictates the N-polar nature of the firstly grown GaN monolayer islands and consequently, the overgrown crystal. As a conclusion, this series confirmed that within the growth temperature range of 900–1150 °C typical for GaN layers, direct growth at higher temperatures result in lower coalescence and growth of vertical micro-hexagonal structures with a large degree of N-polarity, while GaN growth at lower temperatures result in coalesced layers but lower degree of N-polarity and lower crystal quality.

5. Effect of V/III Ratio

We further proceeded with reproducing again our best sample in the temperature series (grown at 1000 °C) showing narrowest linewidth and highest layer coalescence, however, using the V/III ratios of 1100 and 45. As shown in Fig. 5, the lower V/III ratio enhances layer coalescence to a very large extent, while the opposite behavior is observed for higher V/III ratios. The thickness of the coalesced layer grown using the V/III ratio of 45 was measured using optical interference reflectance to be 170 nm. In high resolution X-ray diffraction, the values of 1600 arcseconds and 1550 arcseconds were measured for

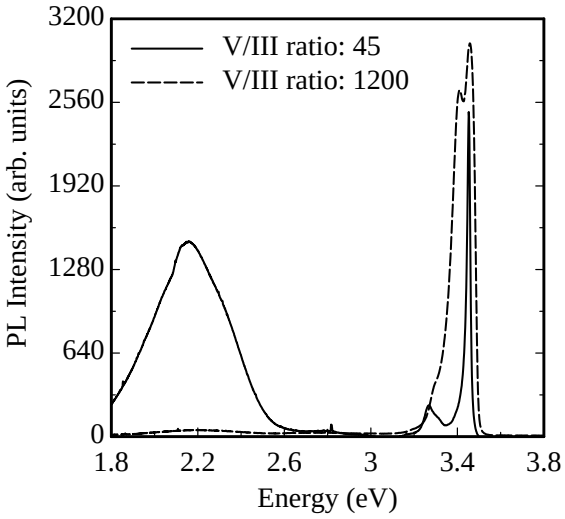

Fig. 6: LT-PL spectra of GaN grown for 10 minutes directly on nitridated sapphire at 1000 °C with V/III ratios of 1100 and 45.

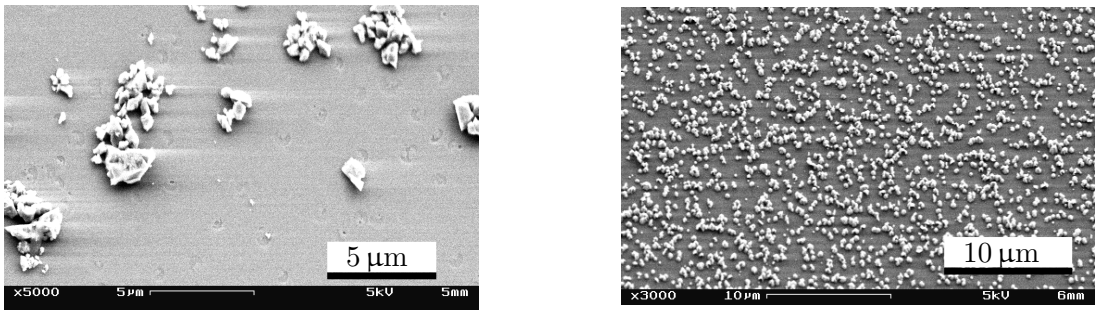

Fig. 7: SEM pictures of GaN grown for 10 minutes directly on nitridated sapphire at 1000 °C under V/III ratios of 45 (left) and 1100 (right) after etching in aqueous KOH solution.

the symmetric (0002) and asymmetric (102) reflections, respectively. It is expected that the latter values will improve to large extents if the layer thicknesses are above[2] 2 µm. Moreover, a narrower linewidth of 20 meV is measured for the totally coalesced layer with V/III ratio of 45 (Fig. 6). However, the latter sample showed stronger yellow luminescence which is assumed to result from atomic vacancies due to reduced supply of ammonia. In addition, the GaN grown at higher V/III ratio showed a strong emission around 3.41 eV indicating the presence of basal plane stacking faults[3] [8]. After the KOH test, more etching of the grown GaN is observed for the sample grown under higher V/III ratio (Fig. 7). Therefore, we conclude that high N precursor supply during nucleation is necessary for the realization of N-polar crystal orientation in the layer. This investigation showed that direct GaN growth under very low V/III ratios enhances lateral growth and layer coalescence, but results in a lower degree of N-polarity.

[2]A thicker layer around 750 nm grown using same conditions (not shown here) revealed the values of 920 arcseconds and 840 arcseconds for the symmetric (0002) and asymmetric (102) reflections, respectively, however with very high surface roughness. Investigations are ongoing for further optimization of surface roughness and crystal quality.

[3]However, in c-plane growth basal plane stacking faults are typically not critical, as they are aligned in the c-plane and hence get buried at larger layer thickness.

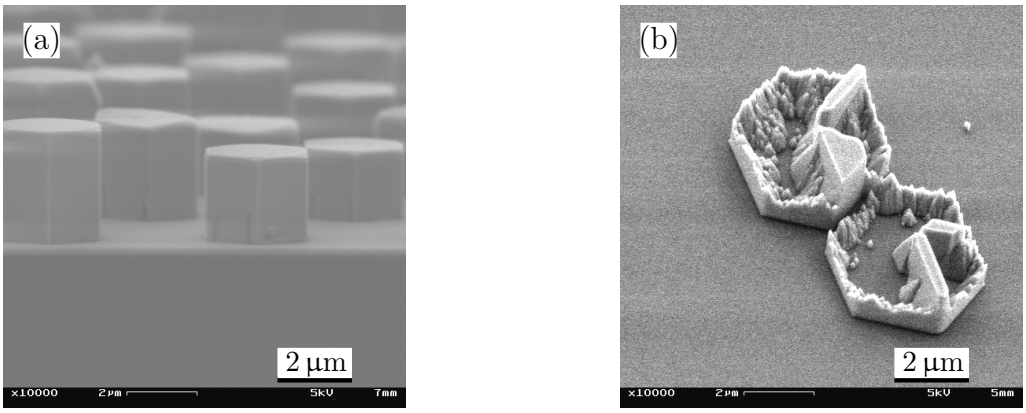

Fig. 8: Selectively grown GaN micro-rods on patterned sapphire using an SiO_2 mask before (a) and after (b) etching in aqueous KOH solution.

6. Selective Area Epitaxy of N-polar GaN

As reported in [4], selectively grown N-polar GaN structures on masked substrates typically favor vertical growth with non-polar planes developing as side facets. This is in comparison to pyramidal structures with semi-polar side facets typically observed for Ga-polar selectively grown GaN. Thus, we wanted to test our growth conditions for GaN layers on a masked sapphire substrate for realizing the afore-mentioned N-polar vertically grown hexagons. We have chosen the same parameters described in Table 1 with a temperature of 1110 °C and a V/III ratio 160 on sapphire substrate masked with 100 nm SiO_2 with circular openings of 3 µm diameter[4]. As shown in Fig. 8 (a), the expected vertical growth was achieved. The KOH test showed that most of the vertically grown micro-structures were etched (Fig. 8 (b)). However, GaN with lower etch rates was still observed within the micro-rods, indicating the existence of inversion domain boundaries. The vertical growth of the selectively grown GaN rods further confirmed that the growth procedure described in Table 1 leads to GaN growth with predominantly N-polar crystal orientation.

7. Conclusion

We have investigated the influence of temperature, nitridation and V/III ratio on the polarity, quality and coalescence of thin nucleation GaN layers (around 170 nm) on c-plane sapphire by metal organic vapor phase epitaxy (MOVPE). It was shown that higher temperatures (above 1100 °C) result in lower coalescence and growth of vertical micro-hexagonal structures with a large degree of N-polarity, while lower temperatures (below 950 °C) resulted in coalesced layer but lower degree of N-polarity and lower crystal quality. Moreover, initial nitridation of the sapphire before GaN growth proved to be critical for achieving N-polar growth and improving the crystal quality. A lower V/III ratio (below 50) at a temperature of 1000 °C showed complete layer coalescence and a linewidth of

[4]The high temperature was chosen to enhance the degree of N-polarity of the selectively grown GaN structures.

20 meV for the GaN band-edge emission, whereas a higher V/III ratio of 1100 resulted in GaN structures separated from one another. Finally, vertical GaN micro-rods selectively grown on patterned sapphire were mostly etched in aqueous KOH solution proving the dominant N-polar exhibiting mainly N-polar growth.

Acknowledgment

We like to thank I. Schwaiger for her assistance with sample processing.

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Realization of Nitrogen-Polar GaN Micro- and Nanostructures

Dominik Heinz and Mohamed Fikry

We report on the selective area growth of N-polar GaN micrometer and sub-micrometer sized structures on structured sapphire wafers for applications in optical gas sensing. Optical lithography has been applied for patterning a SiO_2-mask on the micrometer scale, whereas electron-beam lithography has been used on the nanometer scale. Subsequently, prismatically shaped GaN rods have been fabricated by selective area metal organic vapor phase epitaxy (MOVPE) and first experiments for the realization of GaInN quantum wells on the facets of such structures have been made.

1. Introduction

Today, nanowires find strong interest in research due to their potential applications as light emitting diodes [1], nanolasers [2], as well as single photon emitters and detectors [3, 4]. Morerover, interdisciplinary applications beyond classical optoelectronics are increasingly investigated in particular sensor systems for biomolecules [5], DNA [6], liquids or gases [7, 8]. Due to their large surface to volume ratio, nanowires are in general predestinated as sensing devices [9]. Due to their large bandgap in particular GaN nanostructures are promising candidates for optical gas sensing [10], and furthermore provide a good thermal, chemical, and mechanical stability.

Such a sensing mechanism may be based on the adsorption of oxidative or reductive atoms on the surface which introduces a band bending in the semiconductor which is well understood for ZnO nanowires [11]. This effect corresponds with a change in the photoluminescence emission which in particular can be visible for nanoresonator structures with quantum wells located close to the surface. Uniformly arranged GaN nanowires have been achieved previously within our group by overgrowing ZnO nanowires grown on micrometer-scale GaN pyramids [12]. During this overgrowth the ZnO template desorbs and allows the realization of GaN nanotubes with an even higher surface to volume ratio. However, the inavoidable Zn-doping of GaN in this approach is disadvantageous for potential optical devices with integrated GaInN quantum wells [12].

In this work, we investigate a new approach by growing GaN nanopyramids and nanorods directly on structured sapphire substrates without using a ZnO template. GaN nanorods grow preferably with nitrogen-polarity, while Ga-polar GaN in general results in pyramidal structures [9]. Here, the N-polarity of GaN is achieved by an in-situ nitridation of the sapphire substrate in a hot ammonia atmosphere before growth [13]. During this nitridation step a thin AlN nucleation layer is formed from the Al_2O_3 substrate [14] which

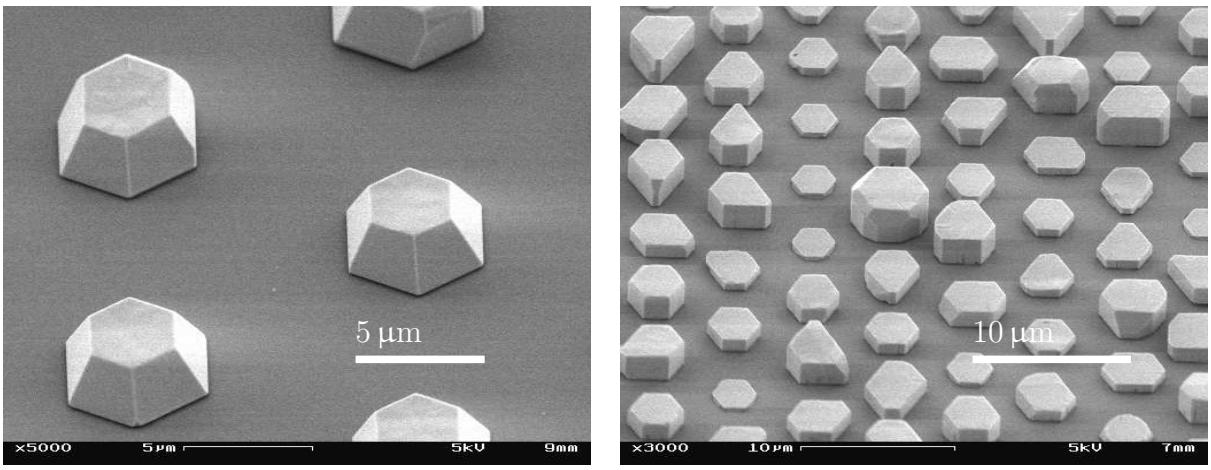

Fig. 1: SEM micrographs of GaN micrometer structures grown on structured sapphire substrates, with a V/III ratio of ≈ 230 (left) and a V/III ratio of ≈ 160 (right).

is then overgrown with nitrogen-polar GaN rods. Moreover, investigations on nitrogen-polar GaN layers have been performed (see the article by M. Fikry in this Annual Report). These buffer layers shall be applied as templates for growth of homogeneously arranged, high quality nanowires. Here, an improved crystal quality and a high fraction in nitrogen-polarity is expected compared to structures directly grown on sapphire.

2. Fabrication

All structures are realized on *c*-oriented sapphire wafers using an horizontal flow Aixtron MOVPE reactor.

For the realization of micrometer sized structures, a thin SiO_2 layer has been deposited onto the sapphire by plasma enhanced chemical vapor deposition. Subsequently, a photoresist layer has been patterned by optical lithography on the SiO_2. Then, reactive ion etching (RIE) with a CF_4 plasma has been applied to etch a hole mask with an opening diameter of 3 µm and a period of 3 µm and 10 µm into the SiO_2, corresponding to a filling factor of approximately 21% and 93% respectively. Finally, in-situ nitridation in hot ammonia and selective area MOVPE at 1100°C has been applied to grow GaN rods. A mixture H_2:N_2 of 2 : 1 has been used as carrier gas during growth.

In case of nanometer sized structures, a spin-coated PMMA layer and subsequent electron-beam lithography has been applied for the etching-mask pattering. Then, holes with a diameter of approximately 100 nm and periods in the µm-range have been etched into the SiO_2 by RIE.

3. Micrometer Rods

For realization of GaN rods a low V/III ratio [1] of approximately 160 and high temperatures of approximately 1110°C were necessary in order to suppress the stable $(10\bar{1}1)$ side facet (compare Fig. 1). This is different than growth conditions for three-dimensional

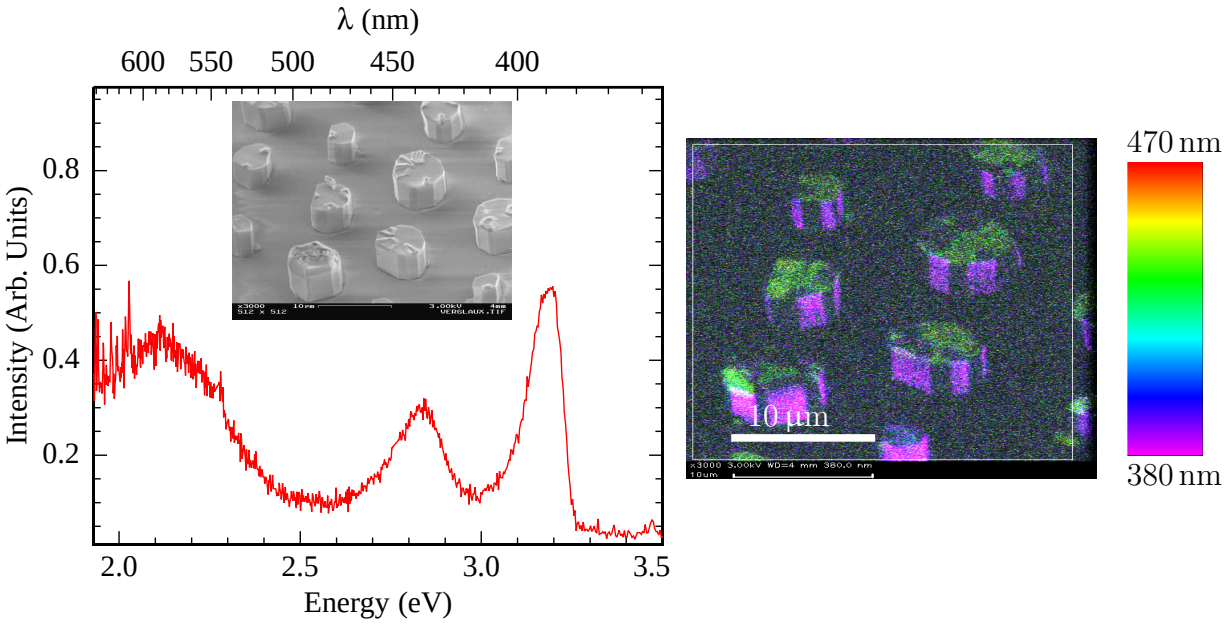

Fig. 2: Low temperature cathodoluminescence measurements of GaN microrods with integrated GaInN quantum well have been performed by I. Tischer at Ulm University. Integrated sprectrum (left) and spatially resolved map (right) demonstrating two contributing kinds of quantum wells located at the top and at the side facets of the structures.

Ga-polar structures where a lower temperature of $\approx 950°C$ and a higher V/III ratio of ≈ 250 is required [15]. The introduction of an in-situ nitridation is crucial for achieving prismatically shaped N-polar structures. In case of pure hydrogen as carrier gas a reduced selectivity, but an improved vertical growth was observed. This can be contributed to the more efficient cracking of NH_3 in pure hydrogen which results in a higher V/III ratio in contrast to the diluted carrier gas. Especially for very high V/III ratios of approximately 1000 no selective growth was observed, which is different to the expected behaviour of Ga-polar GaN structures.

However, while good hexagonal homogeneity in shape was observed for structures with inclined side facets (Fig. 1, left), prismatic structures show a reduced accuracy to the hexagonal shape and stronger height differences (Fig. 1, right). This reduced accuracy can be attributed to the circular mask openings, which in contrast to pyramidal structures apparently show a stronger influence for prismatically shaped structures. However, photoluminescence shows relatively good crystal quality with a FWHM of 42 meV for the near bandedge luminescence located at 3.465 eV.

Subsequently, structures with an additional GaInN quantum well have been realized. Low temperature cathodoluminescence measurements have been performed on both kinds of structures (Fig. 2). In contrast to structures without quantum wells, two additional spectral contributions could be observed at approximately 2.8 and 3.2 eV, which can be attributed to quantum wells located at the c-plane like top of the rods and in addition quantum wells located at the m-plane side facets.

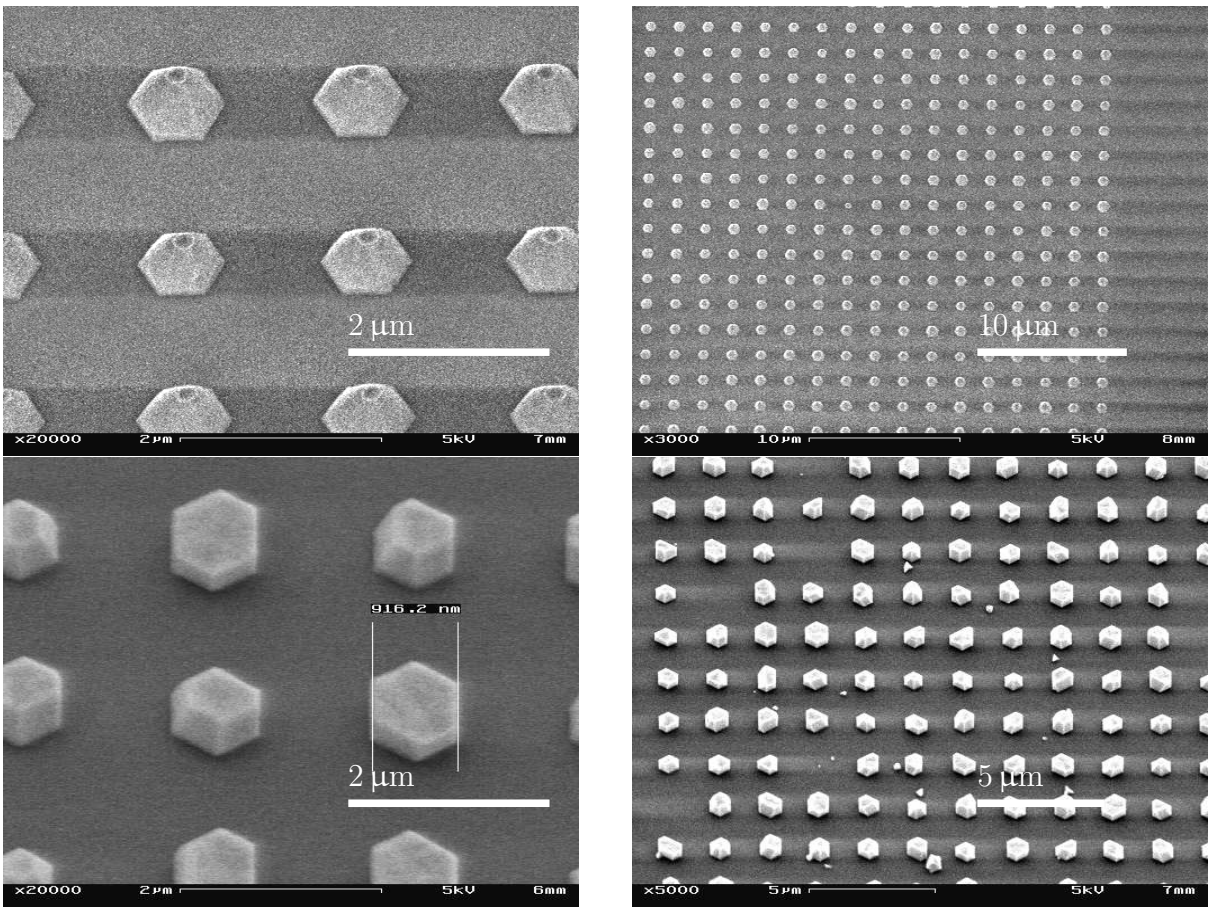

Fig. 3: SEM micrographs of GaN pyramids (top) and rods (bottom) grown on structured sapphire substrates.

4. Sub-Micrometer Rods

The realization of GaN nanowires requires a significant reduction in the diameter of the realized rods and additionally an improved vertical growth rate. In particular, applications as nanoresonators require small dimensions in the range of the investigated wave length. Therefore, the epitaxial process has been transferred from the micro to the nanometer scale by using electron beam lithography. Realized GaN sub-micrometer pyramids and rods are given in Fig. 3.

Good selectivity as well as a homogeneous developement of semipolar $(10\bar{1}1)$ side facets was achieved for pyramidal structures. In constrast, GaN rods show good selectivity in their arrangement. However, inhomogeneities are observed in their hexagonal shape similar to the micrometer structures. As for the micrometer structures, a very low V/III ratio of approximately 100 has been adjusted for growth, not including the additional reduction in the V/III ratio by the high filling factor of the mask with approximately 99.9%. In order to enable an optical read-out of individiual rods in µ-PL with different gas atmospheres a large period of 2 µm was chosen. The observed diameter of the structures lies in the range of 900 nm and therefore requires further reduction.

5. Summary

In this work the realization of GaN rods on the micrometer as well as sub-micrometer scale has been investigated. Instead of using foreign templates like ZnO nanowires, vertical growth was directly achieved on sapphire substrates. Here, selectivity and homogeneity could be significantly improved by adjusting growth parameters while N-polarity was achieved by introduction of an in-situ nitridation step. GaInN quantum wells could be successfully deposited on the side facets of micrometer structures and spatially identified by low temperature cathodoluminescence. In future, in particular the vertical growth rate will be further enhanced to promote the growth of wires with high aspect ratios.

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Combining High-Resolution TEM on Graphene With In-Situ Hall Measurements

Benedikt Westenfelder

We describe an approach allowing high-resolution transmission electron microscopy (HRTEM) on specimens like graphene and the investigation on their electronic transport properties at the same time. The experimental set-up presented here is based on the modification of a commercial TEM specimen holder and on a specially designed sample carrier. A customized Hall sensor confirms that the local magnetic field provided by the microscope's objective lens is sufficiently high and homogenous for in-situ Hall effect measurements. Finally, we discuss first experimental results on defective graphene specimens. Indeed, our data reveals great potential in terms of correlating the information which we gain from HRTEM images with the corresponding transport properties, but also indicates further tasks and challenges.

1. Introduction

Not later then 2010, when the Nobel Prize went to Andre Geim and Konstantin Novoselov, the novel material graphene, basically a single atomic layer of hexagonally arranged carbon atoms, got well known for it's large number of outstanding properties [1]. Without further ado, it could be called the thinnest material on earth providing highest mechanical stability at the same time. Due to its very low thickness it is also extremely transparent (only 2.3 % broadband absorption) and interestingly, it is still an exceptionally good conductor [2,3]. For instance, it provides mobilities of $1.2 \cdot 10^5\,\mathrm{cm}^2/(\mathrm{Vs})$ near room temperature ($T = 240\,\mathrm{K}$) and relatively high sheet carrier densities of $2 \cdot 10^{11}\,\mathrm{cm}^{-2}$ [4]. Even if its surface its not functionalized, i.e., if its surface could be considered as chemically inert, its very large surface-area-to-volume ratio provides large potential for sensing applications [5, 6]. The excellent sensing functionality has been confirmed experimentally several times, however without detailed understanding in terms of the real interaction mechanisms behind. It shouldn't be only a matter of quantifying the actual number of adsorbed molecules: As known from theoretical studies, smallest changes on their detailed atomic position can be induced by different temperatures and affect the electronic interaction differently [7]. This ranges from small shifts of the Fermi level to significant modifications of the intrinsic electronic band structure, i.e., the formation of a band gap. The same holds when we consider defects instead of a perfect graphene lattice. The transport properties, i.e., the carrier mobility, might strongly depend on the number and the sort of defects. Here, we could distinguish roughly between grain boundaries originating inevitably from the growth process or even intentionally implanted point defects, e.g., in order to modify the transport properties [8]. The latter is the sort of defect which we

have chosen for illustrating our approach. In terms of a proof-of-principle approach, we demonstrate how imaging on an atomic scale with simultaneous transport measurements could be performed for revealing deeper insights into the world of defects and their role on the transport properties.

2. Experimental Requirements

The specimens were studied by aberration-corrected HRTEM (AC-HRTEM) performed by a TITAN (80-300) FEI microscope at only 80 kV to avoid knock-on damage [9]. In order to induce intentional defects the microscope has been switched to 300 kV in between and switched back to 80 kV for imaging. Changes on the electronic properties in terms of the sheet resistance have been investigated according to the Van der Pauw method (see ref. [10]) via in-situ four-point probe electrical measurements. Once the magnetic field of the microscope's objective lens had been determined, also the carrier concentration and the Hall mobility could be evaluated.

2.1 The microscope's 'internal' field

We fabricated a specially designed Hall sensor in order to determine the microscope's 'internal' magnetic field (induced by the objective lens) at 80 kV operation (Fig. 1a). The sensor itself consists of a $8 \times 8\,\mu m^2$ mesa structure based on a 1 µm thick n-doped GaAs top layer grown on semi-insulating GaAs (Fig. 1b). Its tiny dimensions have been chosen in order resolve possible magnetic field variations with correspondingly high spatial resolution. The mesa is located centrally to four electrical contact pads. After mounting the Hall sensor into an appropriate TEM specimen holder, the Van der Pauw method has been applied for ex-situ calibration and subsequently for in-situ scanning of the magnetic field at all possible specimen positions. The field was found to be considerably homogeneous corresponding to 1.224 T±0.001 T at 80 kV.

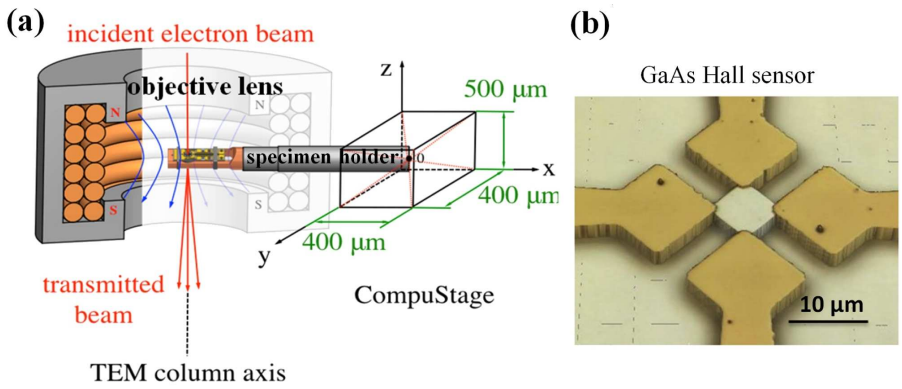

Fig. 1: (a) Scheme of the measurement concept. The magnetic field gets monitored for all possible specimen positions. (b) Three-dimensional (3D) confocal optical micrograph of the GaAs-based mesa structure and its four contact electrodes.

2.2 TEM specimen holder

Our single tilt heating holder from Gatan, Inc. (Model 628) provides six electrical feedthroughs for in-situ electrical experimentation accessible via six metallic pins located behind the actual specimen location (Fig. 2a). However, it still requires some modifications in order obtain feasible access to four wires at least — any wire-bonding-based solution would be too delicate. For this reason, we added a ceramic plate that includes four U-shaped metal sticks bridging the large distance between pins and specimen location (Fig. 2b). The small metal sticks are guided and stabilized by an insulating ceramic ring. The sticks also act as spring contacts when the Hall sensor gets mounted upside down and fixed by a hollow lock screw.

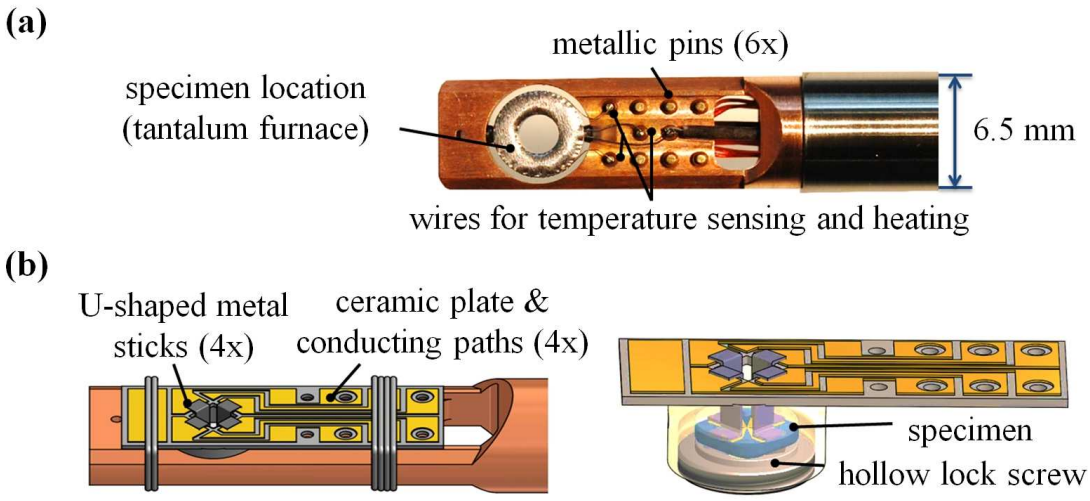

Fig. 2: (a) Photograph of the original front part of the specimen holder. (b) Front part after adding a ceramic plate with embedded conducting paths and four U-shaped metal sticks.

2.3 Graphene specimen

Just as for the Hall sensor, also the graphene specimens must provide large contact areas and fulfill standard TEM specimen size requirements. The specimens here are based on a silicon frame covered with an insulating SiN_x top layer of 750 nm (Fig. 3a). Furthermore, each specimen has a SiN_x window that includes a central opening. This is the area of interest for HRTEM imaging. On top of that opening, the graphene membrane is be suspended between four electrodes. The electrodes (200 nm) have been embedded into the SiN_x top layer in order to avoid topography-induced curvatures resulting in strain. The graphene samples (single layers and bilayers) are fabricated via mechanical exfoliation. After transferring the graphene on top of the electrodes [11], we applied optical lithography and reactive ion etching in order to obtain a fully freestanding graphene structure. The electrode pitch has been chosen as small as possible in order to avoid large fragileness and the necessity of critical point drying. The pitch corresponds to 1.5 µm — small enough, but close to the limit which can be achieved with optical lithography (Figs. 3b,c).

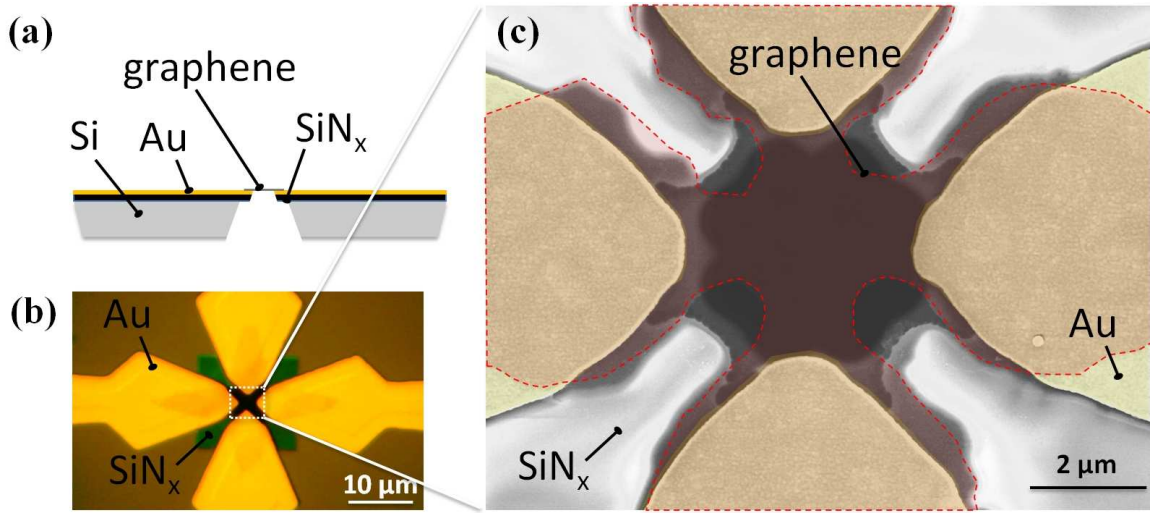

Fig. 3: (a) Schematic diagram of the graphene specimen. (b) Optical micrograph of the real specimen (central part). (c) SEM micrograph of the real specimen (central part) revealing the lithographically patterned graphene sheet.

3. Experiments

After the specimen preparation and a final cleaning procedure in various organic solutions, the graphene surface remains highly contaminated, not visibly but on the microscopic scale. This amount of residues typically changes electronic properties so drastically that the mobility is reduced by even two orders of magnitude. However, a clean initial condition is required in order to correlate structural changes like defects on the atomic scale with a change in the electronic transport properties.

In order to remove all residues, the sample (graphene bilayer) has been pre-annealed in the TEM column by applying a heating function integrated into the specimen holder. The sample has been baked gently at 200 °C for 1 hour resulting already in a significant increase of the mobility ($314\,\mathrm{cm^2/(Vs)}$ to $1708\,\mathrm{cm^2/(Vs)}$) and decrease of the carrier concentration ($3 \cdot 10^{-12}\,\mathrm{cm^{-2}}$ to $4 \cdot 10^{-12}\,\mathrm{cm^{-2}}$). So, the mobility has now been interpreted as an indicator for the sample's cleanness. We might expect a rather clean sample now, but first images revealed still a large degree of contamination. Apparently the annealing temperature was not high enough.

It has been found, once a contaminated sample has been irradiated, i.e., imaged, the residues cannot be driven off anymore. For this reason, we had to use new samples for another pre-annealing at *higher* temperatures. This time, not the entire specimen, but only the freestanding graphene membrane gets heated via Joule heating. This happened via driving a current through the graphene flake. The current annealing procedure has the advantage of achieving temperatures until the regime of 2000 K [12]. There is only one difficulty: we do not have a direct measure for the local temperature, but just a rough idea by the electrical power that is consumed by the membrane. Furthermore, it is not possible to watch/irradiate the sample during the annealing procedure. So there is a large risk of damaging the membrane by small cracks or even the full destruction

of the sample. In order to reach temperatures close to 2000 K considering our specific membrane geometry, a constant bias of approximately 2 V has been applied between two electrodes pairs. Each pair consists of two neighboring electrodes that are switched in parallel. During biasing, an increase of the current can be observed, corresponding to the desorption of residues.

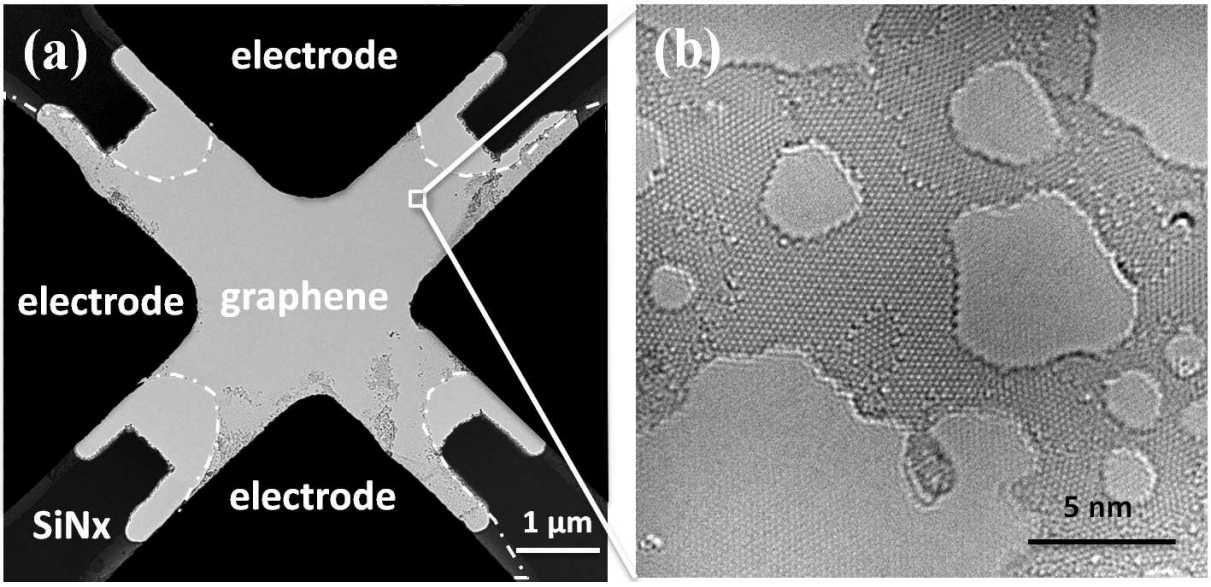

Fig. 4: (a) TEM overview image. The graphene membrane is indicated by the white broken line. It appears clean, apart from visible gray spots at the boundary. These small regions correspond to 3D carbon residues. (b) The HRTEM image reveals the presence of additional two-dimensional graphene patches. Again, they can be found only at the membrane's boundary. The underlying graphene lattice was removed applying a Fourier filter.

After a saturation of that behavior, the annealing has been considered to be finished and the membrane has been imaged for the first time (Fig. 4). Indeed, aside from few impurities at the boundary, the membrane appeared very clean. As also known from former experiments [13], the HR images reveal graphene patches formed on top of the graphene membrane. They are distributed on large areas along the membrane's entire boundary while the central membrane area appeared to be atomically clean. Interestingly, the in-situ transport measurements do not show a significant improvement on mobility compared to the previous experiment at gentle heating. At which extent the graphene patches may influence the transport measurement is not clarified yet. However, the formation of the graphene patches must originate from last residues that are rather present at the areas close to the gold electrodes. Due to increased heat dissipation, the temperature might be slightly lower there compared to the central region. We may speculate that the transformation of those potentially mobile hydrocarbons residues into fixed additional graphene layers occurs too fast for being able to drive them off. Obviously, obtaining the ideal temperature considering an appropriate annealing time is difficult. Furthermore, in contrast to single layer graphene, there is no experimental room temperature mobility value established in the literature for freestanding bilayer graphene. So it remains uncertain, which value should be expected after the successful application of Joule heating.

In order to investigate relative changes on the transport properties by implanted defects, the mobility does not necessarily need to be exceptionally high. For those investigations, we now consistently applied single layer graphene membranes. In order to avoid additional graphitic layers or damage by overheating, we do not exceed an annealing bias of 2.0 V. Furthermore, the annealing has to be interrupted after 30 min for practical limitations (limited microscope operation time). In order to avoid any redeposition of water molecules, we applied a constant background temperature of 175 °C by activating the integrated heating function of the specimen holder. This is important, because the high energetic beam electrons are able to crack potentially adsorbed water molecules into free radicals of hydrogen and oxygen. Those can easily initialize chemical etching processes accompanied with the systematic perforation of the graphene membrane. Finally, when we started the implantation of defects at 300 kV, we continually measured the mobility, the carrier density and the sheet resistance. Sometimes, our measurements showed considerable fluctuations. Normally, this could be correlated with the observation of forming holes or cracks. We also obtained similar fluctuations directly after increasing the dose rate, but without recognizing any visible change on the graphene membrane. Fig. 5a shows a HRTEM image of the graphene surface taken after 100 min of irradiation.

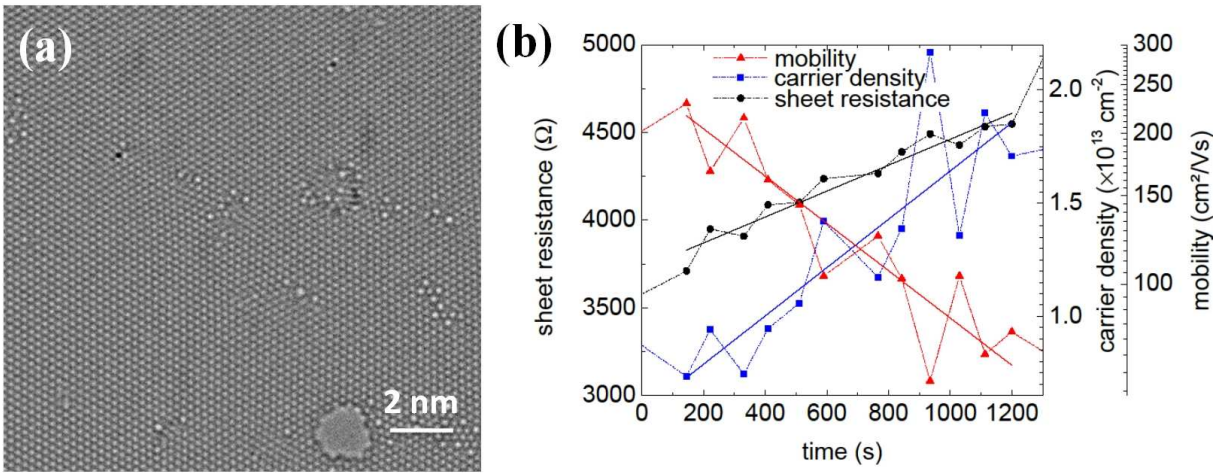

Fig. 5: (a) HRTEM image of the irradiated graphene membrane revealing a large number of defects. (b) Time-dependent behavior of the transport properties while irradiating constantly with $3.2 \cdot 10^8\, e\, \mu m^{-2} s^{-1}$ at 300 kV, with e being the electron charge.

Only time segments belonging to constant conditions, i.e., not during crack formations or changes on the dose rate, can be used for reasonably interpreting the measured transport properties. Such section is shown in Fig. 5b. As expected, during the defect implantation time, we find an exponential decay of the mobility and an increase of the sheet resistance. This suggests an increase of defect induced scattering processes. However, we also find an increase of the carrier density. As known from gate operated graphene devices [4], also the increasing number of carriers could be responsible for the decay in the mobility. The most probable origin of the increasing number of charge carriers might be the incorporation of impurity atoms into the defective sites [14].

4. Conclusions and Outlook

In summary, we presented an approach allowing the correlation between HRTEM imaging and the transport properties on a very basic level. At first, we discussed the realization of the most relevant technical issues, i.e., the magnetic field, the specimen holder and the sample carrier. Finally, we introduced one sample application demonstrating how directly visualized defective sites can be correlated to the electronic transport properties.

Further studies, i.e., density functional theory based simulations of the experimentally obtained defect distributions might help to clarify at which extent the decrease in mobility can be related purely to an increased lattice disorder and at which extend changes in the carrier density (most likely by doping on defective sites) has to be considered. The conversion from defective graphene into fully amorphized graphene is basically a matter of the electron dose and the irradiation time [15]. Our approach could help to clarify from the experimental perspective if such amorphized graphene specimens behave rather metallic or insulating [16–18].

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Ph.D. Theses

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