Investigations of GaN-Based Vertical Field Effect Transistors for Applications in High-Power Electronics

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In this report, some pre-studies for our research project "Investigations of GaN-based vertical field effect transistors (FETs) for applications in high-power electronics" will be shown. In particular, we have re-established decent hydride vapor phase epitaxy sample quality as confirmed by Hall, high-resolution X-ray diffraction and as well by mercury probe measurements. In addition we started with the growth of classical two-dimensional FET test structures by metal organic vapor phase epitaxy.

1. Introduction

For large power density while simultaneously enabling high power conversion efficiency and reduced form factor in semiconductor devices, GaN is a very promising material [1]. However, with ever increasing power density in two-dimensional devices, one reaches a critical source-drain voltage before avalanche-like breakthrough occurs [2] due to free charge carriers accumulating near the gate on the drain side [3]. Current devices work around this issue by increasing the distance between gate and drain contacts [3]. However, these devices need ever increasing space in the horizontal plane. By using the third dimension, it is possible to hold the blocking voltage for still small lateral dimensions. One possible approach is the so-called current aperture vertical electron transistor (CAVET) as shown in Fig. 1. In addition to the decreased lateral size of a three-dimensional-transistor, the problem of surface charges is reduced, as the active region is located within the material [3].

The way these devices work is the following: The field-effect control of the current is very similar as in conventional lateral devices high electron mobility transistors (HEMTs): The gate voltage controls the two-dimensional carrier gas density at the AlGaN-GaN interface. Below this interface, an insulating blocking-layer prevents carriers from escaping to the bulk. The electrons flow from the source contact to the region below the gate where the blocking layer is interrupted thus forming a current aperture. Hence the carriers can drift down to the drain contact positioned below the current aperture. Consequently, fairly large gate-drain distances and thus blocking voltages can be realized by the thickness of this drift region without compromising the lateral size of the device. Therefore, it is possible to control high currents with the gate voltage, while large source-drain voltages can be applied [1, 4].

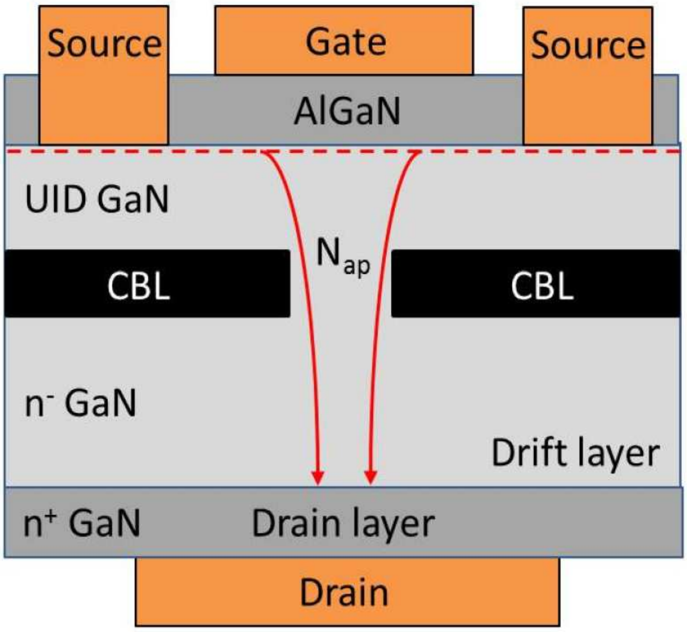

Fig. 1: Schematic view of a CAVET. On top, a classical HEMT structure with an AlGaN layer on unintentionally doped GaN for high electron mobility in the two-dimensional carrier gas at the interface, then the current blocking layer (CBL) forming the current aperture and channelling the current, next a thick drift layer, holding the blocking voltage, and at the bottom a higher n-doped layer for the drain contact (after [1]) .

For such a device to work, it is important to have good crystal quality, otherwise threading dislocations can penetrate the current-blocking layer and create an unwanted current path, the region under the gate being particularly critical. Also for high breakdown voltages, a low free charge carrier concentration is required in the drift region. Therefore, such devices are typically grown on free-standing GaN wafers grown by hydride vapor phase epitaxy (HVPE).

For preparing structures for such CAVETs, we worked on re-establishing good crystal quality in HVPE and metal organic vapor phase epitaxy (MOVPE) grown samples.

2. Experimental Details

The HVPE reactor used to grow thick GaN samples is a horizontal, five-zone hot-wall showerhead reactor (Aixtron Aix LP VPE). A mixture of nitrogen and hydrogen is used as carrier gas, while ammonia is used as the group-V precursor. As Ga precursor, gallium-chloride is formed in-situ by streaming gaseous hydrochloric acid (HCl) over a pure gallium bath at 850 °C. The growth is performed on 2-inch, 2 µm thick MOVPE grown GaN layers on sapphire similar as described by Scholz *et al.* [8].

For the MOVPE growth, a low-pressure horizontal reactor (Aixtron AIX-200/4 RF-S) with the Aixtron standard 2-inch SiC-coated graphite suszceptor is used. All samples are grown on standard (0001) sapphire substrates with an offcut of 0.3° towards the m-plane. Trimethyl-aluminium (TMAl), trimethyl-gallium (TMGa) and ammonia are used as precursors.

For characterisation, a high-resolution X-ray diffractometer (Bruker Discover D8) is used to check the crystal quality of the samples. From the measured rocking curve full-width-half-maximum (FWHM) data, the dislocation density can be deduced [5]. We used a pinhole of 0.3 mm on the emitter side in order to reduce the unwanted effect of peak broadening due to wafer curvature. A Hall setup with a magnetic field of 0.45 T was used to determine carrier concentration and mobility. For our test structures, contacts made of 5 nm titanium, 220 nm aluminium, 40 nm nickel and 50 nm gold have been deposited. The contacts were annealed at 700 °C for three minutes.

Capacitance-voltage (C-V) measurements were performed using a mercury probe at Inatech in Freiburg by M.Sc. Björn Christian.

3. Growth and Evaluation of HVPE and MOVPE Test Samples

Currently, high quality GaN layers with a reasonable thickness of 2 µm grown in our MOVPE reactor have typical X-ray diffraction rocking curve widths of 300 arcsec and 400 arcsec for the symmetric (002) and the asymmetric (102) peak, respectively, as confirmed by high-resolution X-ray diffraction (HRXRD) measurements. It is expected that the defect density and hence the FWHM of the rocking curve peaks is reduced in thicker layers grown on such templates by HVPE. However, in these studies, we concentrated on fairly thin HVPE layers of about 15 µm thickness in order to keep them crack-free. Indeed, most samples show slight improvement in crystal quality for the 102 peak which mainly reflects edge-type dislocations. For the best samples, we found peak widths as low as 200 arcsec. The 002 peak, mainly caused by screw-type dislocations, typically did not change significantly. One possible explanation for this is the fact that because of the different growth speed in the HVPE as compared to the MOVPE we get a more three-dimensional growth an therefore the stacking of the crystal planes is not so good in the c-direction. Another possible explanation for the still high defect density may be due to the not yet perfectly optimized HVPE process. On some samples, we found particles from the shower head which might disturb the further growth. A better cleaning procedure with HCl may help to overcome such problems.

It is important to note here that, even though we did not see a clear reduction in the 002 FWHM, the defect density scales with the square of the respective FWHM for the respective peak. Therefore a factor two in the 102 peak width means a significant reduction in dislocation density of the samples by a factor of four [5].

In order to directly confirm the improved crystal quality and to get quantitative values for the dislocation density, it is planned to measure the etch pit density of the samples and calculate from that the number of threading dislocations reaching the surface.

This can be done by etching the samples in the HVPE reactor at elevated temperatures with HCl [6]. The etch pit density can then be determined either by scanning electron microscopy or by atomic force microscopy.

The electrical characteristics of our MOVPE and HVPE layers were measured via the use of the Hall effect in van-der-Pauw geometry. The carrier concentration of the 2 µm thick MOVPE samples was below the detection limit of our setup. For the 15 µm thick HVPE samples, n-type carrier concentrations in the order of $2 \cdot 10^{16}\,\mathrm{cm}^{-3}$ were measured.

On three MOVPE and two HVPE samples, C-V profiles were measured using a mercury probe at Inatech (University of Freiburg). These experiments confirmed the quite low carrier concentration in these samples: The free-carrier concentration for all except one HVPE sample was not high enough for the measurement, indicating good quality and a useful substrate for further applications in vertical field effect transistors. Only one sample was near the detection limit of the C-V-measurement (Fig. 2).

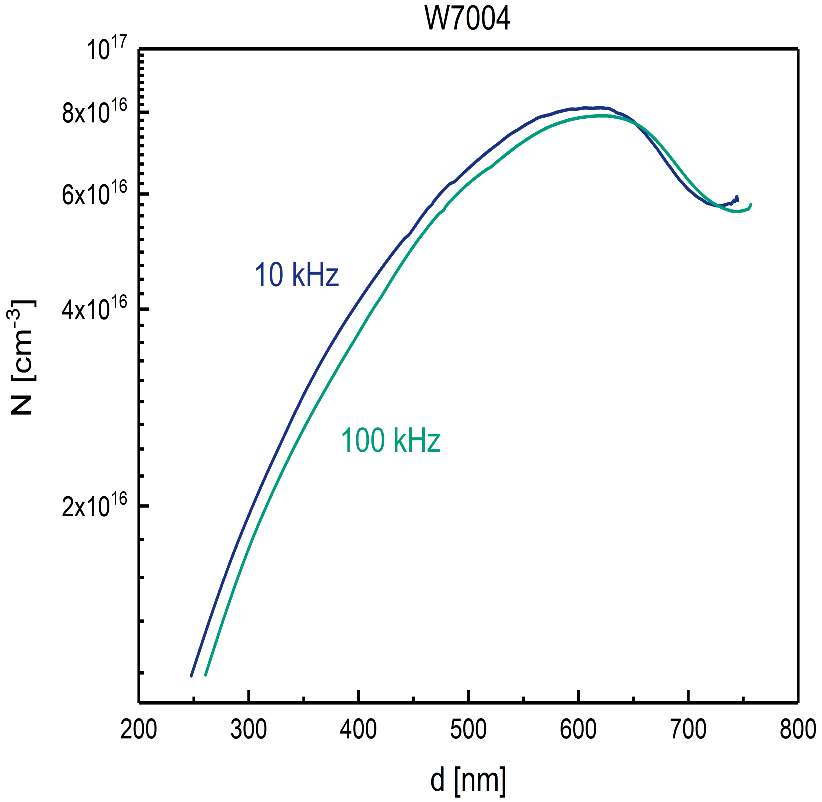

Fig. 2: C-V depth scan near the surface of a 15 µm thick HVPE sample (W7004) for two different measurement frequencies, showing a slight deviation from the carrier concentration of $4.8 \cdot 10^{16}\mathrm{cm}^{-3}$ measured by Hall. This is probably due to the fact that in Hall the bulk data is measured while C-V measurements are surface-sensitive. Even though the sample was near the detection limit, a meaningful depth profile could be obtained, since the courses for the two different measurement frequencies are similar .

4. Growth and Evaluation of 2-D HEMTs Grown in MOVPE

In addition to the HVPE experiments, we started growing classical HEMT test structures by MOVPE being composed of an AlGaN barrier on top of our undoped GaN layers described above, where a 2-dimensional electron gas (2DEG) is formed at the boundary between GaN and AlGaN.

Starting with a sapphire wafer, first 2 µm thick GaN was grown. On top of that a 18 nm thick $Al_{0.34}Ga_{0.66}N$ barrier layer was deposited and finally a 3 nm thick GaN cap layer for better contacts. Between the AlGaN and the GaN layer an about 1 nm thick AlN layer was placed which prevents the electron wave function to penetrate into the ternary barrier and thus leads to a higher mobility of the 2DEG.

These first test structures show promising results with an electron mobility of $1326\,\mathrm{cm^2/(Vs)}$ at room-temperature and $4328\,\mathrm{cm^2/(Vs)}$ at 77 K. The fairly low values at nitrogen temperature indicate that we still have some defects in our layers which requires further optimization. However the measured carrier concentration of $1.9 \cdot 10^{13}\,\mathrm{cm^{-2}}$ is high when compared to expected results for such structures [7].

A possible explanation for this may be unintentional doping [9]. However since our buffer layers have indicated high resistivity, the doping might come from the AlN precursor TMAl.

5. Summary

In order to improve the breakdown voltages of GaN-based field effect transistors, we have started to investigate the concept of vertical transistors. For such devices, high quality GaN is needed. Therefore we have investigated the quality of MOVPE and HVPE grown GaN layers. HRXRD, Hall-effect and C-V measurements confirmed the high quality of such layers which should be sufficient for vertical transistors. In a next step, etch experiments in our HVPE reactor will be done to determine the defect density directly. First two-dimensional HEMT test structures grown by MOVPE also indicated promising quality for the future device, although the measured sheet carrier concentration is a little bit too high for our purposes, which will also be worked on in the future.

6. Acknowledgment

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