

August 1986 Revised February 1999

DM74LS191 Synchronous 4-Bit Up/Down Counter with Mode Control

General Description

The DM74LS191 circuit is a synchronous, reversible, up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a LOW-to-HIGH level transition of the clock input, if the enable input is LOW. A HIGH at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is HIGH. The direction of the count is determined by the level of the down/up input. When LOW, the counter counts up and when HIGH, it counts down.

The counter is fully programmable; that is, the outputs may be preset to either level by placing a LOW on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words. Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

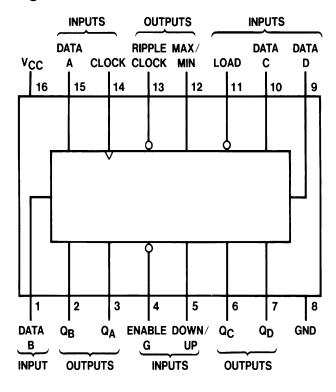
- Counts binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Ordering Code:

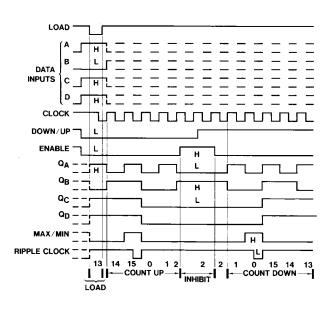
Order Number	Package Number	Package Description			
DM74LS191M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body			
DM74LS191N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

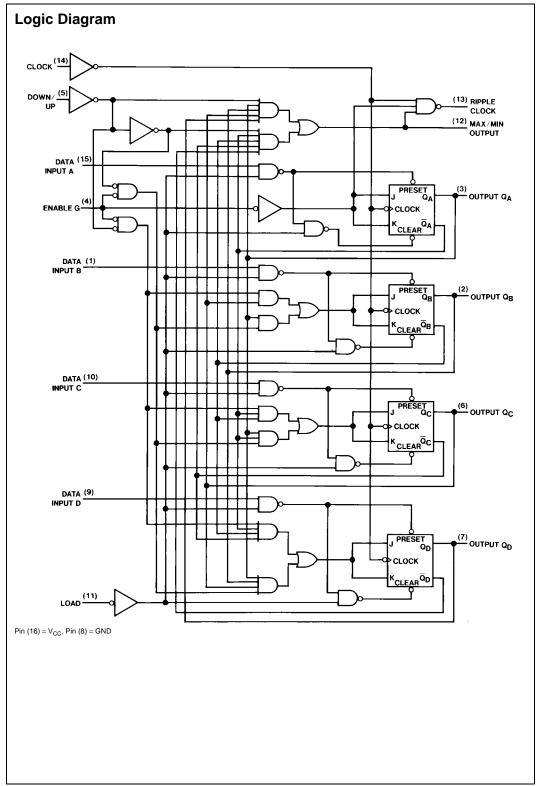
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Timing Diagram





Absolute Maximum Ratings(Note 1)

Storage Temperature Range -65°C to +150°C Input Voltage

Operating Free Air Temp. Range

Supply Voltage 7V

5°C to +150°C

7V

O°C to +70°C

0°C to +70°C

7V

To "Recommended Operating Conditions" table will define the conditions to the conditions the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V _{CC}	Supply Voltage			5	5.25	V
V _{IH}	HIGH Level Input Voltage		2			V
V _{IL}	LOW Level Input Voltage				0.8	V
I _{OH}	HIGH Level Output Current				-0.4	mA
I _{OL}	LOW Level Output Current				8	mA
f _{CLK}	Clock Frequency (Note 2)		0		20	MHz
t _W	Pulse Width	Clock	25			ns
	(Note 2)	Load	35			
t _{SU}	Data Setup Time (Note 2)	•	20			ns
t _H	Data Hold Time (Note 2)		0			ns
t _{EN}	Enable Time to Clock (Note 2)		30			ns
T _A	Free Air Operating Temperature		0		70	°C

Note 2: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

DC Electrical Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Units
					(Note 3)		
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output	V _{CC} = Min, I _{OH} = Max	Mil	2.5	3.4		
	Voltage	$V_{IL} = Max, V_{IH} = Min$	Com	2.7	3.4		V
V _{OL}	LOW Level Output	V _{CC} = Min, I _{OL} = Max			0.25	0.4	
	Voltage	$V_{IL} = Max, V_{IH} = Min$			0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min			0.25	0.4	
I _I	Input Current @ Max	V _{CC} = Max	Enable			0.3	mA
	Input Voltage	$V_I = 7V$	Others			0.1	
I _{IH}	HIGH Level Input	V _{CC} = Max	Enable			60	μА
	Current	$V_I = 2.7V$	Others			20	
I _{IL}	LOW Level Input	V _{CC} = Max	Enable			-1.08	mA
	Current	$V_I = 0.4V$	Others			-0.4	
Ios	Short Circuit	V _{CC} = Max	Mil	-20		-100	mA
	Output Current	(Note 4)	Com	-20		-100	
I _{cc}	Supply Current	V _{CC} = Max (Note 5)			20	35	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25$ °C.

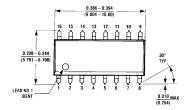
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

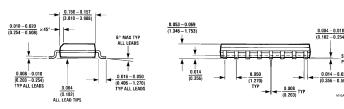
Note 5: I_{CC} is measured with all inputs grounded and all outputs open.

AC Electrical Characteristics

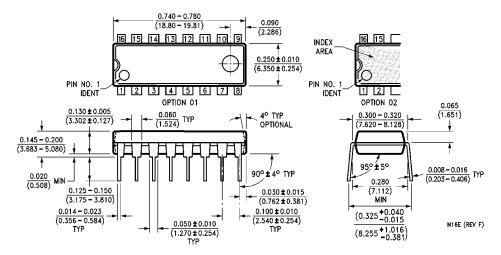
Symbol	Parameter	From (Input) To (Output)					
			C _L = 15 pF		C _L = 50 pF		Units
			Min	Max	Min	Max	1
f _{MAX}	Maximum Clock		20		20		MHz
	Frequency						
t _{PLH}	Propagation Delay Time	Load to		33		43	ns
	LOW-to-HIGH Level Output	Any Q					
t _{PHL}	Propagation Delay Time	Load to		50		59	ns
	HIGH-to-LOW Level Output	Any Q					
t _{PLH}	Propagation Delay Time	Data to		22		26	ns
	LOW-to-HIGH Level Output	Any Q					
t _{PHL}	Propagation Delay Time	Data to		50		62	ns
	HIGH-to-LOW Level Output	Any Q					
t _{PLH}	Propagation Delay Time	Clock to		20		24	ns
	LOW-to-HIGH Level Output	Ripple Clock					
t _{PHL}	Propagation Delay Time	Clock to		24		33	ns
	HIGH-to-LOW Level Output	Ripple Clock					
t _{PLH}	Propagation Delay Time	Clock to		24		29	ns
	LOW-to-HIGH Level Output	Any Q					
t _{PHL}	Propagation Delay Time	Clock to		36		45	ns
	HIGH-to-LOW Level Output	Any Q					
t _{PLH}	Propagation Delay Time	Clock to		42		47	ns
	LOW-to-HIGH Level Output	Max/Min					
t _{PHL}	Propagation Delay Time	Clock to		52		65	ns
	HIGH-to-LOW Level Output	Max/Min					
t _{PLH}	Propagation Delay Time	Up/Down to		45		50	ns
	LOW-to-HIGH Level Output	Ripple Clock					
t _{PHL}	Propagation Delay Time	Up/Down to		45		54	ns
	HIGH-to-LOW Level Output	Ripple Clock					
t _{PLH}	Propagation Delay Time	Down/Up to		33		36	ns
= :	LOW-to-HIGH Level Output	Max/Min					
t _{PHL}	Propagation Delay Time	Down/Up to		33		42	ns
:=	HIGH-to-LOW Level Output	Max/Min					
t _{PLH}	Propagation Delay Time	Enable to		33		36	ns
= :	LOW-to-HIGH Level Output	Ripple Clock					
t _{PHL}	Propagation Delay Time	Enable to		33		42	ns
	HIGH-to-LOW Level Output	Ripple Clock					

Physical Dimensions inches (millimeters) unless otherwise noted





16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS012, 0.150" Narrow Body Package Number M16A



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 300" Wide Package Number N16E

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